APPLICATION MANUAL

RV-4162

Ultra Small

Real Time Clock / Calendar Module

with I2C Interface

A COMPANY OF THE SWATCH GROUP

Headquarters:
Micro Crystal AG
Mühlestrasse 14
CH-2540 Grenchen
Switzerland

Tel. +41 32 655 82 82
Fax +41 32 655 82 83
Internet www.microcrystal.com
Email sales@microcrystal.com

TABLE OF CONTENTS

RV-4162

Ultra Small Real Time Clock / Calendar Module with I²C Interface

1. OVERVIEW

- RTC module with built-in “Tuning Fork” crystal oscillating at 32.768 kHz
- Serial RTC with alarm functions:
  - 400 kHz I²C serial interface
  - Memory mapped registers for seconds, minutes, hours, day, date, month, year and century
  - Tenths / hundredths of seconds register
- 350 nA timekeeping current at 3.0 V
- Timekeeping down to 1.0 V
- 1.3 V to 4.4 V I²C bus operating voltage
- Low operating current of 35 μA (f_{SCL} = 400 kHz)
- 32.768 kHz square wave output available at power-up, suitable for driving a uC in low power mode (can be disabled)
- Programmable 1 Hz to 32.768 kHz square wave output
- Programmable alarm with interrupt function
- Oscillator stop detection monitors clock operation
- Accurate programmable watchdog: 62.5 ms to 31 min timeout
- Software clock calibration, can adjust timekeeping within +/-2 ppm
- Automatic leap year compensation
- Operating temperature range: -40°C to +85°C
- Ultra small and compact C7 package size, RoHS-compliant and 100% leadfree: 3.2 x 1.5 x 0.8 mm

1.1. GENERAL DESCRIPTION

The RV-4162 is a low power serial Real Time Clock (RTC) module with built-in 32.768 kHz crystal (no external components are required for the oscillator). Eight registers are used for the clock / calendar function and are configured in binary coded decimal (BCD) format. An additional 8 registers provide status / control of alarm, calibration, programmable square wave output and watchdog functions. Addresses and data are transferred serially via a two line, bidirectional I²C interface. The built-in address register is incremented automatically after each WRITE or READ data byte.

Functions available to the user include a time-of-day clock / calendar, alarm interrupts, programmable square wave output, and watchdog. The eight clock address locations contain the century, year, month, date, day, hour, minute, second and tenths / hundredths of a second in 24-hour BCD format. Corrections for 28, 29 (leap year), 30 and 31 day months are made automatically.

1.2. APPLICATIONS

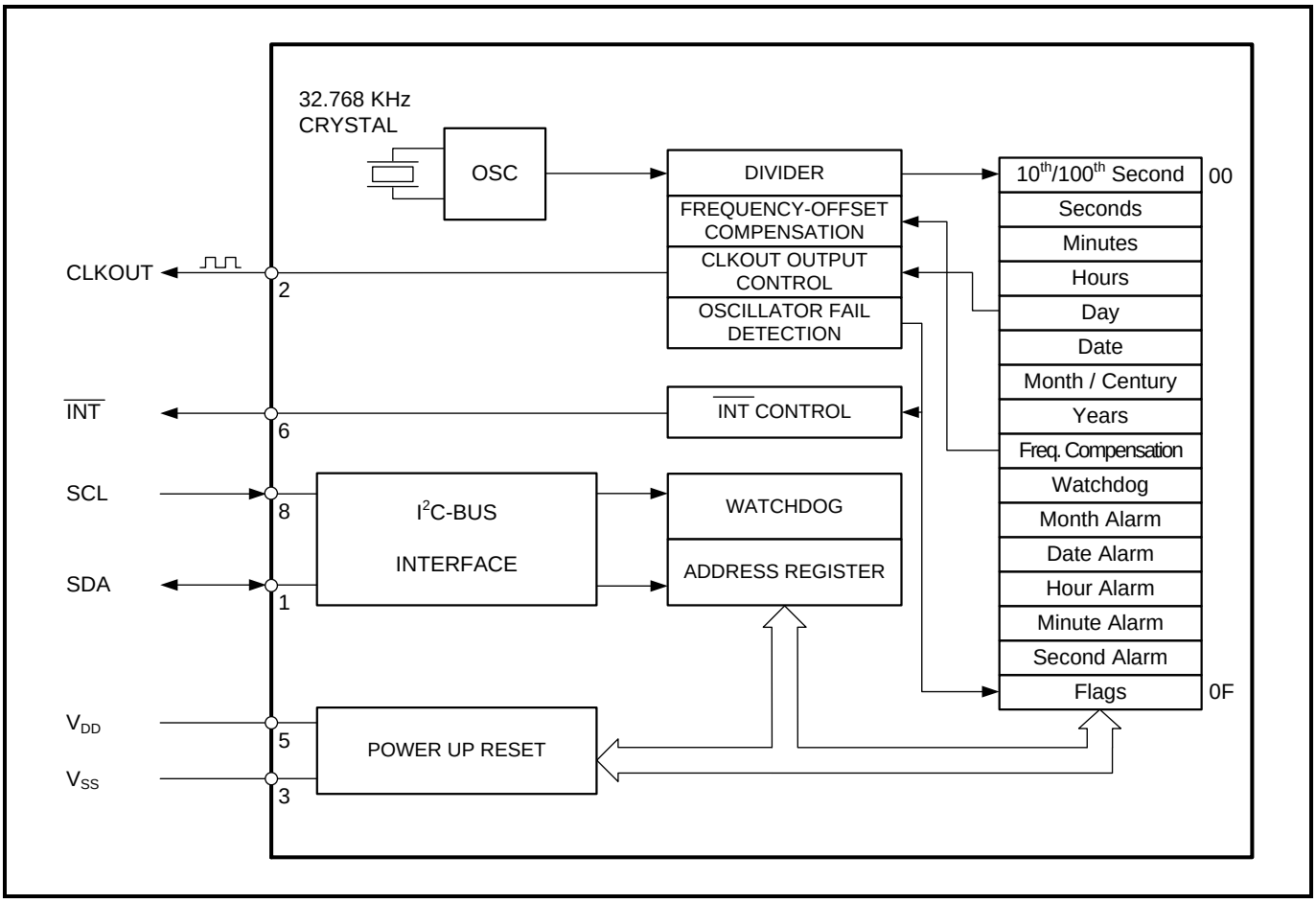
The RV-4162 RTC module combines standard RTC functions in high reliable, ultra-small ceramic package:

- Smallest RTC module (embedded XTAL) in an ultra-small 3.2 x 1.5 x 0.8 mm leadfree ceramic package.
- Price competitive

The unique size and the competitive pricing make this product perfectly suitable for many applications:

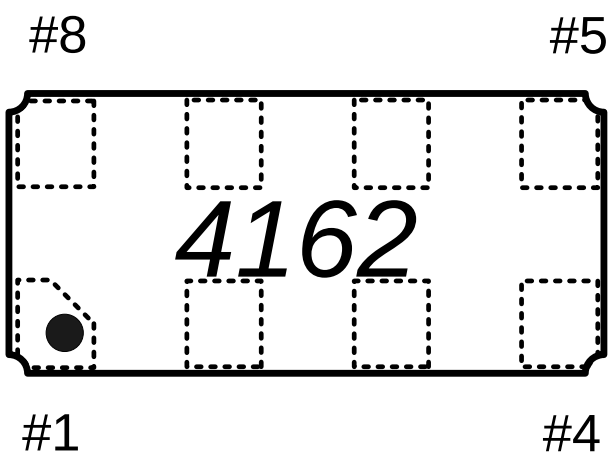
- Automotive: Navigation & Tracking Systems / Dashboard / Tachometers / Car Audio & Entertainment Systems
- Metering: E-Meter / Heating Counter / Smart Meters / PV Converter
- Outdoor: ATM & POS systems / Ticketing Systems
- Medical: Glucose Meter / Health Monitoring Systems
- Safety: Security & Camera Systems / Door Lock & Access Control
- Consumer: Gambling Machines / TV & Set Top Boxes / White Goods
- Automation: Data Logger / Home & Factory Automation / Industrial and Consumer Electronics

2. BLOCK DIAGRAM



2.1. PINOUT

C7 Package:



#1	SDA	#8	SCL
#2	CLKOUT	#7	N.C.
#3	V_{SS}	#6	$\overline{INT}$
#4	N.C.	#5	V_{DD}

2.2. PIN DESCRIPTION

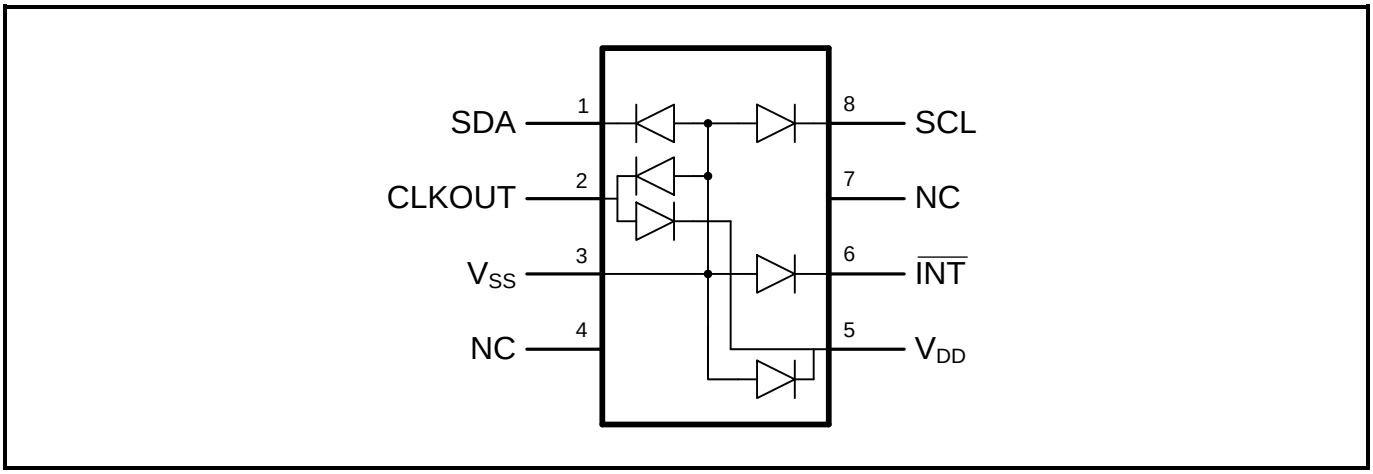
Symbol	Pin #	Description
SDA	1	Serial Data; open-drain; requires pull-up resistor
CLKOUT	2	Clock Output
V_{SS}	3	Ground
N.C.	4	Not Connected
V_{DD}	5	Power Supply Voltage
$\overline{INT}$	6	Interrupt Output; open-drain; requires pull-up resistor; active low
N.C.	7	Not Connected
SCL	8	Serial Clock Input; requires pull-up resistor

2.3. FUNCTIONAL DESCRIPTION

The RV-4162 is a low power CMOS Real-Time Clock / Calendar module with built-in “Tuning-Fork” crystal with the nominal frequency of 32.768 kHz; no external components are required for the oscillator circuitry.
The oscillator frequency on all devices is tested not to exceed a time deviation of ± 20 ppm (parts per million) at 25°C, which equates to about ± 52 seconds per month.
This time accuracy can be further improved to ± 2 ppm at 25°C or better by individually measuring the frequency-deviation in the application and programming a correction value into the frequency compensation register.

The CMOS IC contains 16 8-bit RAM registers; the address counter is automatically incremented after each written or read data byte. All sixteen registers are designed as addressable 8-bit parallel registers, although, not all bits are implemented.

2.4. DEVICE PROTECTION DIAGRAM



3. REGISTER ORGANIZATION

The RV-4162 user interface consists of 16 memory mapped registers which include clock, calibration, alarm, watchdog, flags, and square wave control.

First 8 registers are the Clock Section at address 00h through 07h. These registers are accessed indirectly via a set of transfer registers.

Clock Section (addresses 00h through 07h):

These registers are coded in BCD format and contain the century, year, month, day / date, hours, minutes, seconds and tenths / hundredths of seconds in 24-hour format. Corrections for 28, 29 (leap year), 30 or 31 day of months are made automatically. These registers are accessed indirectly through transfer registers.

Next 8 registers are the control section at address 08h through 0Fh.

Control Section (addresses 08h through 0Fh):

These registers are coded in binary format and provide status, frequency compensation, alarm and control of the peripheral functions including the programmable clock output and watchdog functions.

The CMOS IC contains 16 8-bit RAM registers. These registers are carried out double: internal counters and external user accessible registers.

All sixteen registers are designed as addressable 8-bit parallel registers, although, not all bits are implemented. The address counter is automatically incremented after each written or read data byte.

The internal registers keeping track of the time based on the 32.768 kHz clock oscillator and the divider chain. The external registers are independent of the internal counters except that they are updated periodically by the simultaneous transfer of the incremented internal data. To prevent data transition during Interface access, the content of the external register is kept stable whenever the address being read is a clock address (00h to 07h). The update of the external register will resume either when the address-pointer increments to a non-clock address or Interface communication is terminated by sending a “STOP condition”.

After “WRITE” to the external register, when the “STOP condition” terminates the Interface communication, the content of the modified external registers is copied into the corresponding internal registers. The divider chain of the 32.768 kHz oscillator will be reset upon the completion of a “WRITE” to any clock address (00h to 07h).

3.1. REGISTER ACCESS

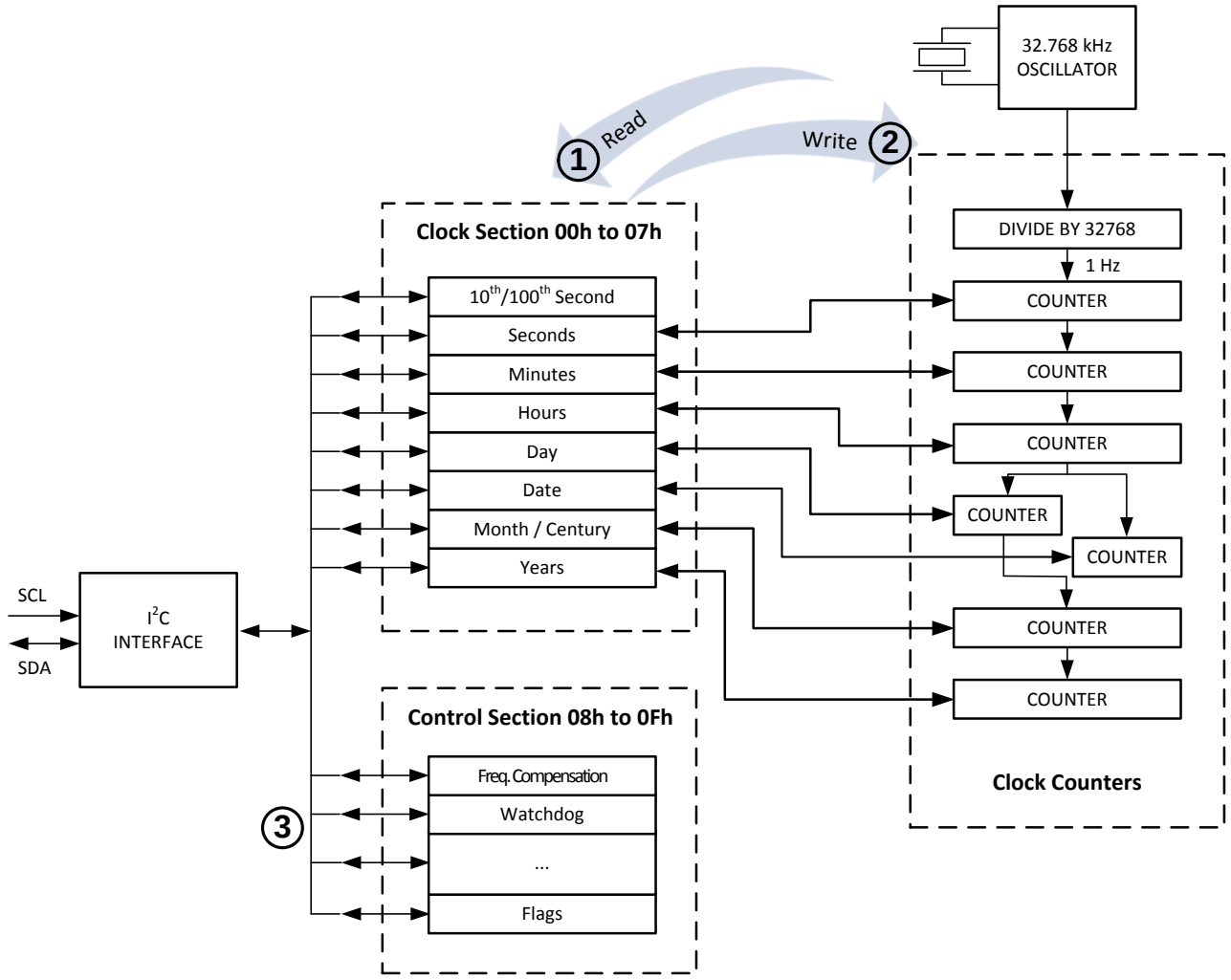
During normal operation when the user is not accessing the device, the transfer registers are kept updated with a copy of the Clock Counter data.

At the start of an I^2C read or write cycle, the updating is halted and the present time & date is frozen in the transfer registers. Halting the updates at the start of an I^2C access is to ensure that all the time & date data transferred out during a read sequence comes from the same instant in time.

When writing to the device, each bit is shifted into the RV-4162's I^2C Interface on the rising edge of the SCL signal. On the 8th clock cycle, each byte is transferred from the I^2C block into the register addressed by the address pointer.

Data written to the Clock Registers (addresses 00h - 07h) is held in the transfer registers until the address pointer increments to 08h, or when STOP condition from I^2C Interface is received. At which time the data in the transfer registers are simultaneously copied into the Clock Counters and then the clock is restarted.

3.2. BUFFER / TRANSFER REGISTERS



"Clock Counter Registers" containing time & date information are accessed indirectly through transfer registers.

1 At start of Read command, data from "Clock Counter Registers" are copied into "Transfer Register" and the present time & date is frozen. The I^2C Interface reads the frozen data from Transfer Register, the internal Clock Counter continuous to be updated by the 1 second ticks.

2 When Write to the "Clock Counter Registers", data are written to the "Transfer Register" and internally transferred to the "Clock Counter Registers" when address pointer increments to 08h or when STOP condition from I^2C Interface is received.

3 Non clock registers of the Control Section 08h to 0Fh are directly accessed from I^2C Interface.

3.3. REGISTER OVERVIEW

Clock Section (addresses 00h through 07h):

These registers are coded in BCD format and contain the century, year, month, day / date, hour, minute, second and tenths/hundredths of a second in 24-hour format. Corrections for 28, 29 (leap year), 30 or 31day months are made automatically. These registers are accessed indirectly through transfer registers.

Control Section (addresses 08h through 0Fh):

These registers are coded in binary format and provide status, frequency compensation, alarm and control of the peripheral functions incl. the programmable clock-output and watchdog functions.

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	10^{th} / 100^{th} Second	10^{th} of Second				100^{th} of Second			
		8	4	2	1	8	4	2	1
01h	Seconds	OS	40	20	10	8	4	2	1
02h	Minutes	OFIE	40	20	10	8	4	2	1
03h	Hours	0	0	20	10	8	4	2	1
04h	Day	FD3	FD2	FD1	FD0	0	4	2	1
05h	Date	0	0	20	10	8	4	2	1
06h	Month / Century	CB1	CB0	0	10	8	4	2	1
07h	Years	80	40	20	10	8	4	2	1
08h	Freq. Compensation	OUT	0	Mode	16	8	4	2	1
09h	Watchdog	WD2	WDM4	WDM3	WDM2	WDM1	WDM0	WD1	WD0
0Ah	Month Alarm	AFE	CLKOE	0	10	8	4	2	1
0Bh	Date Alarm	ARM4	ARM5	20	10	8	4	2	1
0Ch	Hour Alarm	ARM3	0	20	10	8	4	2	1
0Dh	Minute Alarm	ARM2	40	20	10	8	4	2	1
0Eh	Second Alarm	ARM1	40	20	10	8	4	2	1
0Fh	Flags	WDF	AF	0	0	0	OF	0	0

Bit positions labelled with 0 should always be written with logic “0”.

3.4. CLOCK SECTION

10^{th} / 100^{th} Second (address 00h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	10^{th} / 100^{th} of seconds[1)]	8	4	2	1	8	4	2	1

Bit	Symbol	Value	Description
7 to 4	10^{th} of second	0 to 9	This register hold the current 10^{th} of second coded in BCD format
3 to 0	100^{th} of second	0 to 9	This register hold the current 100^{th} of second coded in BCD format

[1)] Generation of 100^{th} and 10^{th} of second is derived from the internal clock source 32.768 kHz divided by 328 = 0.010009766 second. A WRITE to any register of the Clock Section 00h to 07h will reset the divider chain of the 32.768 kHz clock and set the 10^{th} / 100^{th} of second = "00". Values other than "00" cannot be written to this register.

Seconds (address 01h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01h	Seconds	OS	40	20	10	8	4	2	1

Bit	Symbol	Value	Description
7	OS	0	32.768 kHz oscillator is enabled and starts within $T_{start} \leq 1$ sec.
		1	32.768 kHz oscillator is disabled (stopped)
6 to 0	Seconds	0 to 59	This register holds the current seconds coded in BCD format

Minutes (address 02h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
02h	Minutes	OFIE	40	20	10	8	4	2	1

Bit	Symbol	Value	Description
7	OFIE	0	Oscillator fail interrupt is disabled
		1	Oscillator fail interrupt is enabled; an interrupt will be issued when an oscillator failure is detected
6 to 0	Minutes	0 to 59	This register holds the current minutes coded in BCD format

Hours (address 03h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
03h	Hours	0	0	20	10	8	4	2	1

Bit	Symbol	Value	Description
7 to 6	X	0	Unused; must be set to "0"
5 to 0	Hours	0 to 23	This register holds the current hours coded in BCD format

Day (address 04h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
04h	Day	FD3	FD2	FD1	FD0	0	4	2	1

Bit	Symbol	Value	Description	Reference
7 to 4	FD0 to FD3	0000 to 1111	FD0 to FD3 bits control CLKOUT frequency 0000 no frequency at CLKOUT 0001 to 1111 select the CLKOUT frequency	See section 4.1
3	X	0	Unused; must be set to “0”	
2 to 0	Weekday	1 to 7	This register holds the current weekday coded in BCD format[1)]	

Weekday	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Sunday	X	X	X	X	0	0	0	1
Monday	X	X	X	X	0	0	1	0
Tuesday	X	X	X	X	0	0	1	1
Wednesday	X	X	X	X	0	1	0	0
Thursday	X	X	X	X	0	1	0	1
Friday	X	X	X	X	0	1	1	0
Saturday	X	X	X	X	0	1	1	1

[1)] These bits may be re-assigned by the user.

Date (address 05h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
05h	Date	0	0	20	10	8	4	2	1

Bit	Symbol	Value	Description
7 to 6	X	0	Unused; must be set to “0”
5 to 0	Date	0 to 31	This register holds the current date coded in BCD format

Month / Century (address 06h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
06h	Month / Century	CB1	CB0	0	10	8	4	2	1

Bit	Symbol	Value		Description	Leap Year
		CB1	CB0		
7 to 6	Century	0	0	Century 20xx (year 2000 – 2099)	2000 = yes
		0	1	Century 21xx (year 2100 – 2199)	2100 = no
		1	0	Century 22xx (year 2200 – 2299)	2200 = no
		1	1	Century 23xx (year 2300 – 2399)	2300 = no
5	X	0		Unused; must be set to “0”	
4 to 0	Month	1 to 12		This register holds the current month coded in BCD format	

Months	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
January	X	X	0	0	0	0	0	1
February	X	X	0	0	0	0	1	0
March	X	X	0	0	0	0	1	1
April	X	X	0	0	0	1	0	0
May	X	X	0	0	0	1	0	1
June	X	X	0	0	0	1	1	0
July	X	X	0	0	0	1	1	1
August	X	X	0	0	1	0	0	0
September	X	X	0	0	1	0	0	1
October	X	X	0	1	0	0	0	0
November	X	X	0	1	0	0	0	1
December	X	X	0	1	0	0	1	0

Years (address 07h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
07h	Years	80	40	20	10	8	4	2	1

Bit	Symbol	Value	Description
7 to 0	Years	0 to 99	This register holds the current year coded in BCD format

3.5. CONTROL SECTION

Frequency Compensation (address 08h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08h	Freq. Compensation	OUT	0	Mode	16	8	4	2	1

Bit	Symbol	Value	Description
7	OUT	0	When OFIE, AFE and Watchdog register are not set to generate an interrupt, the $\overline{INT}$ pin 6 becomes logic output reflecting the content of this bit 7 "OUT"; See section 4.8
		1	
6	X	0	Unused; must be set to "0"
5	Mode	0	Negative calibration; See section 4.2
		1	Positive calibration; See section 4.2
4 to 0	Calibration value	0 to 31	This register holds the calibration value coded in binary format

Watchdog (address 09h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
09h	Watchdog	WD2	WDM4	WDM3	WDM2	WDM1	WDM0	WD1	WD0

Bit	Symbol	Value	Description
7, 1, 0	WD2 / WD1 / WD0	000 - 100	Watchdog Timer Clock Source: 16Hz / 4Hz / 1 Hz / ¼ Hz / $^1/_{60}$ Hz
6 to 2	WDM4 to WDM0	0 to 31	This register holds the binary coded Watchdog Multiplier value

Month Alarm (address 0Ah…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Ah	Month Alarm	AFE	CLKOE	0	10	8	4	2	1

Bit	Symbol	Value	Description
7	AFE	0	Disables Alarm Flag
		1	Enables Alarm Flag
6	CLKOE	0	Disables CLKOUT (clock output pin 2)
		1	Enables CLKOUT (clock output pin 2)
5	X	0	Unused; must be set to "0"
4 to 0	Month alarm	1 to 12	This register holds the month alarm coded in BCD format

Date Alarm (address 0Bh…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Bh	Date Alarm	ARM4	ARM5	20	10	8	4	2	1

Bit	Symbol	Value	Description
7 to 6	ARM4 – ARM5	00 to 11	Alarm repeat mode; See section 4.4
5 to 0	Date alarm	1 to 31	This register holds the date alarm coded in BCD format

Hour Alarm (address 0Ch…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Ch	Hour Alarm	ARM3	0	20	10	8	4	2	1

Bit	Symbol	Value	Description
7	ARM3	0 / 1	Alarm repeat mode; See section 4.4
6	X	0	Unused; must be set to “0”
5 to 0	Hour alarm	0 to 23	This register holds the hour alarm coded in BCD format

Minute Alarm (address 0Dh…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Dh	Minute Alarm	ARM2	40	20	10	8	4	2	1

Bit	Symbol	Value	Description
7	ARM2	0 / 1	Alarm repeat mode; See section 4.4
6 to 0	Minute alarm	0 to 59	This register holds the Minutes Alarm coded in BCD format

Second Alarm (address 0Eh…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Eh	Second Alarm	ARM1	40	20	10	8	4	2	1

Bit	Symbol	Value	Description
7	ARM1	0 / 1	Alarm repeat mode; See section 4.4
6 to 0	Second alarm	0 to 59	This register holds the second alarm coded in BCD format

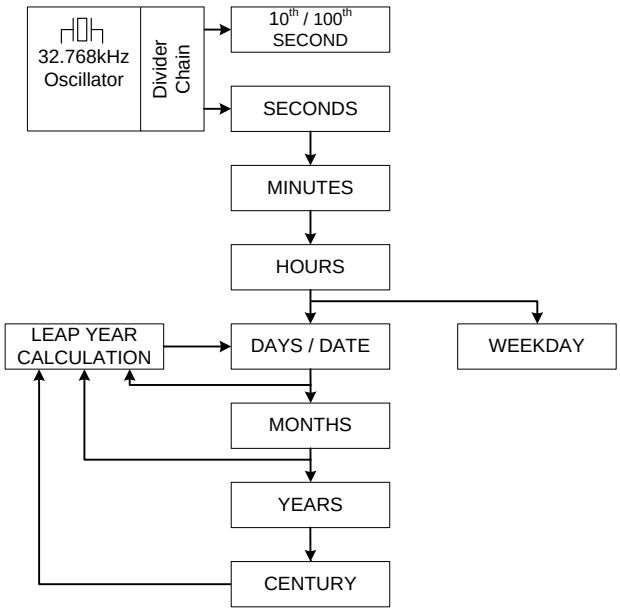
Flags (address 0Fh…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Fh	Flags	WDF	AF	0	0	0	OF	0	0

Bit	Symbol	Value	Description
7	WDF	0	No watchdog timer timeout error detected
		1	Watchdog timer timeout error detected, an interrupt will be generated
6	AF	0	No matching alarm condition detected
		1	Alarm flag set when watch matches Alarm settings If AIE = 1, an alarm interrupt will be generated
5 to 3 and 1 to 0	X	0	Unused; must be set to “0”
2	OF	0	No oscillator failure timeout error detected
		1	Oscillator failure timeout error detected If OFIE = 1, an oscillator fail interrupt will be generated

[1)] WDF and AF are read only bits, will be automatically cleared when read.

3.6. DATA FLOW OF TIME AND DATE FUNCTION



3.7. REGISTER RESET VALUE

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	10th / 100th Second	X	X	X	X	X	X	X	X
01h	Seconds	0	X	X	X	X	X	X	X
02h	Minutes	0	X	X	X	X	X	X	X
03h	Hours	X	X	X	X	X	X	X	X
04h	Day	0	0	0	1	X	X	X	X
05h	Date	X	X	X	X	X	X	X	X
06h	Month / Century	X	X	X	X	X	X	X	X
07h	Years	X	X	X	X	X	X	X	X
08h	Freq. Compensation	1	X	X	X	X	X	X	X
09h	Watchdog	0	0	0	0	0	0	0	0
0Ah	Month Alarm	0	1	X	X	X	X	X	X
0Bh	Date Alarm	X	X	X	X	X	X	X	X
0Ch	Hour Alarm	X	X	X	X	X	X	X	X
0Dh	Minute Alarm	X	X	X	X	X	X	X	X
0Eh	Second Alarm	X	X	X	X	X	X	X	X
0Fh	Flags	X	X	X	X	X	1	X	X

Bit positions labelled as “X” are undefined at power-on and unchanged by subsequent resets.

4. DETAILED FUNCTIONAL DESCRIPTION

4.1. CLKOUT FREQUENCY SELECTION

The RV-4162 offers the user a programmable square wave clock which is available at CLKOUT pin 2. CLKOUT frequency is programmable by bits FD3 - FD0 (bit 7 - 4 in register Day 04h) according to below table:

CLKOUT frequency selection (address 04h…FD3 - FD0 bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
04h	Day	FD3	FD2	FD1	FD0	0	4	2	1

Bit	Symbol	Values				CLKOUT	
		FD3	FD2	FD1	FD0	Frequency	Units
7 to 4	FD3 to FD0	0	0	0	0	None	-
		0	0	0	1	32.768	kHz
		0	0	1	0	8.192	kHz
		0	0	1	1	4.096	kHz
		0	1	0	0	2.048	kHz
		0	1	0	1	1.024	kHz
		0	1	1	0	512	Hz
		0	1	1	1	256	Hz
		1	0	0	0	128	Hz
		1	0	0	1	64	Hz
		1	0	1	0	32	Hz
		1	0	1	1	16	Hz
		1	1	0	0	8	Hz
		1	1	0	1	4	Hz
		1	1	1	0	2	Hz
		1	1	1	1	1	Hz

CLKOUT pin 2 is push-pull output and can be disabled either by setting bits FD3 - FD0 = “0000” or by setting bit CLKOE (bit 6 in register Month Alarm 0Ah) = “0”.

CLKOUT frequency enable / disable (address 0Ah…CLKOE bit description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Ah	Month Alarm	AFE	CLKOE	0	10	8	4	2	1

Bit	Symbol	Value	Description
6	CLKOE	0	Disables CLKOUT (clock output pin 2)
		1	Enables CLKOUT (clock output pin 2)

Default setting at initial power-up is CLKOUT enabled with the frequency of 32.768 kHz. It is recommended to disable CLKOUT when not used by the application to minimize current consumption of the device.

4.2. FREQUENCY OFFSET COMPENSATION

The frequency offset compensation function gives the end user the ability to calibrate the clock and to improve the time accuracy of the RV-4162.

The RTC is clocked by an oscillator operating a quartz crystal resonator with a nominal frequency of 32.768 kHz. The oscillator frequency on all devices is laser-trimmed and tested not to exceed a time deviation of ±20 ppm at 25°C, which equates to about ±52 seconds per month.

The RV-4162 employs periodic clock counter correction. By properly setting the frequency calibration register in the application, it can improve its time accuracy to typically ±2 ppm at 25 °C. The frequency compensation is made by adding or subtracting clock correction counts from the oscillator divider chain at 128 Hz ("divide by 256 stage"), thereby changing the period of a single second.

The number of clock pulses which are subtracted (negative calibration) or added (positive calibration) depends upon the value loaded into the five compensation bits (bit 0 to bit 4) of the Frequency Compensation Register. Adding counts speeds the clock up; subtracting counts slows the clock down.

The frequency offset compensation is controlled by the Frequency Compensation Register 08h. The calibration value occupies the five LSB's (bit 4 - 0). These bits can be set to represent any value between 0 and 31 in binary format. Bit 5 "Mode" is a sign bit; "1" indicates positive calibration and speeds up the time, "0" indicates negative calibration and slows down the time

Freq. Compensation (address 08h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08h	Calibration Register	OUT	0	Mode	16	8	4	2	1

Bit	Symbol	Value	Description
5	Mode	0	Negative calibration; compensates time deviation when 32.768 kHz clock is too fast
		1	Positive calibration; compensates time deviation when 32.768kHz clock is too slow
4 to 0	Calibration value	0 to 31	This register holds the calibration value coded in binary format

	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Compensation Value in Decimal	Frequency Compensation Event	
								Time correction [ppm]	Compensation event
Negative	0	1	1	1	1	1	+31	-63.054	1st- 62nd minute, 1 event each minute
	0	1	1	1	1	0	+30	-61.02	1st - 60th minute, 1 event each minute
			:				:	:	
	0	0	0	0	1	0	+2	-4.068	1st - 4th minute, 1 event each minute
	0	0	0	0	0	1	+1	-2.034	1st & 2nd minute, 1 event each minute
	0	0	0	0	0	0	0[1)]	0	No correction
Positive	1	1	1	1	1	1	-1	+4.068	1st & 2nd minute, 1 event each minute
	1	1	1	1	1	0	-2	+8.138	1st – 4th minute, 1 event each minute
			:				:	:	
	1	0	0	0	0	1	-30	+122.04	1st - 60th minute, 1 event each minute
	1	0	0	0	0	0	-31	+126.108	1st- 62nd minute, 1 event each minute

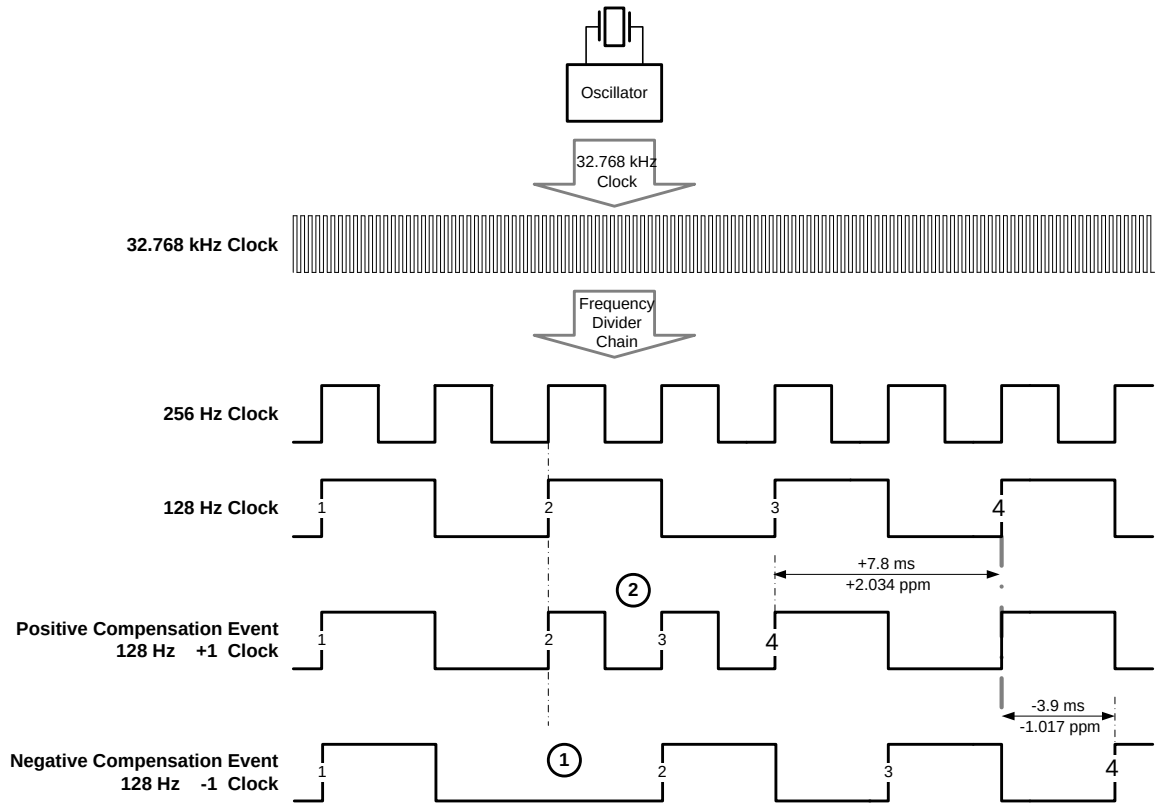
[1)] Default mode at power-up.

4.2.1. FREQUENCY OFFSET COMPENSATION METHOD

The frequency compensation itself occurs within a 64 minute cycle. Each binary coded calibration value will trigger two compensation events; compensation events are applied once per minute until the programmed calibration value has been implemented. If, for example a binary “1” is loaded into the Frequency Compensation Register, only the first 2 minutes in the 64 minute cycle will contain one compensation event each. If a binary ‘6’ is loaded, the first 12 minutes will be affected, and so on.

Each compensation event either shortens one second by 7.8 ms (256 x 32.768 kHz oscillator clock cycles) or lengthened it by 3.9 ms (128 x 32.768 kHz oscillator clock cycles). Therefore, each calibration value triggers two compensation events resulting in a time adjustment of -2.034 ppm (slower by -0.175 seconds per day) or +4.068 ppm (faster by +0.351 seconds per day) for each of the 31 values of the calibration value.

The maximum calibration value (31d) defines the compensation range of -63.054 ppm (slower by -5.449 seconds per day) or +126.108 ppm (faster by +10.899 seconds per day).



(1) **Negative compensation (when 32.768 kHz clock too fast):**
Then for each compensation event, a clock pulse at the 128 Hz divider stage is suppressed to compensate the frequency deviation of the 32.768 kHz clock.

(2) **Positive compensation (when 32.768 kHz clock too slow):**
Then for each compensation event a clock pulse at the 128 Hz divider stage is added to compensate the frequency deviation of the 32.768 kHz clock.

Note that frequency compensation events do not affect the frequency at CLKOUT pin 2.

4.2.2. DEFINING FREQUENCY COMPENSATION VALUE

The simplest method for ascertaining the frequency deviation a given RV-4162 is to measure the frequency deviation at CLKOUT pin 2. The measured frequency deviation, then, is transformed into an individual compensation value for this device and programmed into the Frequency Compensation Register (08h).

For test purpose, the following configuration will establish a 32.768 kHz clock at CLKOUT pin 2:

- Bit OS = “0” (bit 7 in register Seconds 01h): enables 32.768 kHz oscillator
- Bits FD3 – FD0 = “0001” (bits 7 - 4 in register Day 04h): select 32.768 kHz CLKOUT frequency
- Bit CLKOE = “1” (bit 6 in register Month Alarm 0Ah): enables CLKOUT pin 2

Please note that this is the default setting at power-up.

The frequency deviation on 32.768000 kHz CLKOUT indicates the degree and direction of time deviation for this device. A frequency deviation of +0.032768 Hz equals to +1 ppm.

For example, a reading of 32.768650 kHz indicates a frequency deviation of +20 ppm (faster by +1.73 seconds per day), requiring negative compensation value of “-10d” (xx001010) to be loaded into the Frequency Compensation Register (08h) for frequency compensation.

It’s important to define the frequency compensation value at an ambient temperature (around 25°C) because of the crystal’s frequency vs. temperature characteristics shown on page 29.

4.3. WATCHDOG TIMER

The Watchdog Timer can be used to detect an out-of-control microprocessor or deadlock of the Interface communication. The function of the Interface Watchdog Timer is based on internal Timer / Counter which is periodically reset by the internal control logic. If the control logic does not reset the Watchdog Timer within the programmed time-out period, the RV-4162 detects an Interface time-out and sets Watchdog Flag (WDF = 1, bit 7, in register Flags 0Fh) and generates an interrupt on $\overline{INT}$ pin 6.

The user programs the Watchdog Timer by setting the desired amount of time-out into the Watchdog register at address 09h, a value of 00h will disable the watchdog function until it is again programmed to a new value.

The amount of time-out is then determined by selecting a Watchdog Timer Source Clock WD2 - WD0 and the multiplication with the Watchdog Multiplier value WDM4 - WDM0.

- Bits WDM4 - WDM0 store a binary coded Watchdog Multiplier value.
- Bits WD2 - WD0 select the Watchdog Timer Clock Source.

For example: writing 00001110 in the Watchdog register = 3 x 1 second or 3 seconds.

Watchdog (address 09h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
09h	Watchdog	WD2	WDM4	WDM3	WDM2	WDM1	WDM0	WD1	WD0

Bit	Symbol	Value	Description
7 to 0	Watchdog	00h	A value of 00h disables Watchdog Timer function
7, 1, 0	WD2 / WD1 / WD0	000 - 100	Watchdog Timer Clock Source: 16Hz / 4Hz / 1 Hz / ¼ Hz / $^1/_{60}$ Hz
6 to 2	WDM4 to WDM0	0 to 31	This register holds the binary coded Watchdog Multiplier value

WDM4	WDM3	WDM2	WDM1	WDM0	Value	Description
0	0	0	0	0	00h	Setting “00000” with any combination of WD2 - WD0, other than “000”, will result in an immediate watchdog time-out
0	0	0	0	1	01d	Defines binary coded Watchdog Multiplier value
…					…	
1	1	1	1	0	30d	
1	1	1	1	1	31d	

WD2	WD1	WD0	Value	Timer Clock Source	Time
0	0	0	000	16 Hz	62.5ms
0	0	1	001	4 Hz	250 ms
0	1	0	010	1 Hz	1 second
0	1	1	011	¼ Hz	4 seconds
1	0	0	100	$^1/_{60}$ Hz	1 minute
1	0	1	101	Invalid combination, will not enable Watchdog Timer	
1	1	0	110	Invalid combination, will not enable Watchdog Timer	
1	1	1	111	Invalid combination, will not enable Watchdog Timer	

The Watchdog time-out period starts when the I^2C interface communication is initiated. If the control logic does not reset the Watchdog Timer within the programmed time-out period, the RV-4162 detects an Interface time-out and sets the Watchdog Flag (WDF = 1, bit 7, in register Flags 0Fh) and generates an interrupt on $\overline{INT}$ pin 6.

The Watchdog Timer can only be reset by having the microprocessor perform a WRITE to the Watchdog Register 09h. The time-out period then starts over.

Should the Watchdog Timer time-out, any value may be written to the watchdog register in order to clear the $\overline{INT}$ pin 6. A value of 00h will disable the watchdog function until it is again programmed to a new value. A READ of the flags register will reset the Watchdog Flag (bit 7; register 0Fh). The watchdog function is automatically disabled upon power-up, and the Watchdog Register is cleared.

Note: A WRITE to any clock register will restart the Watchdog Timer.

4.4. ALARM FUNCTION

Addresses locations 0Ah-0Eh contain the alarm settings. The alarm can be configured to go off at a prescribed time on a specific month, date, hour, minute, or second, or repeat every year, month, day, hour, minute, or second.

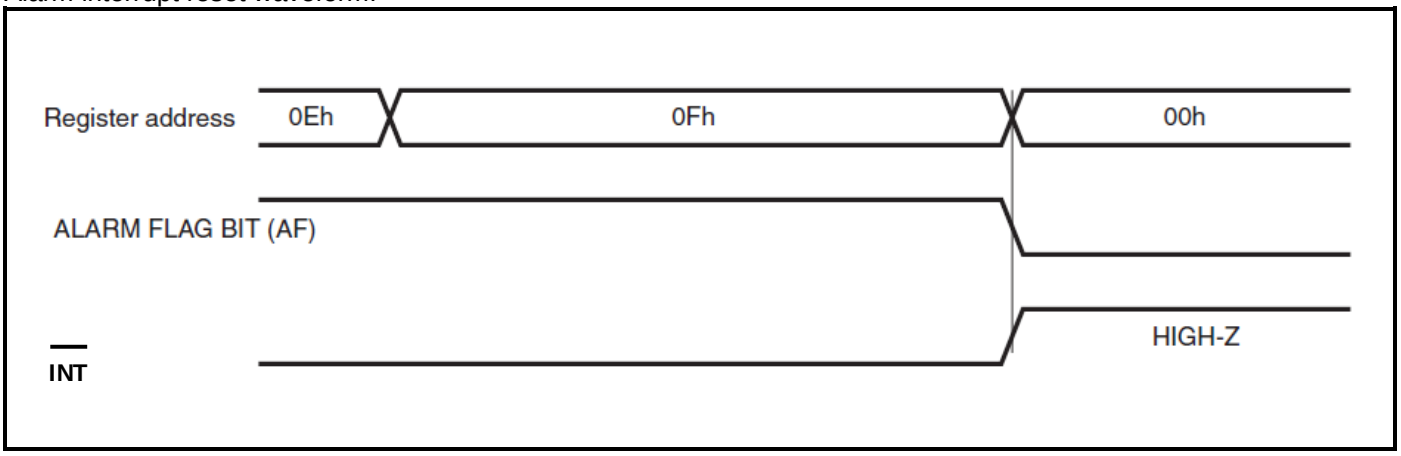
Bits ARM5 - ARM1 put the alarm in the repeat mode of operation. The table below shows the possible configurations. Codes not listed in the table default to the once per second mode to quickly alert the user of an incorrect alarm setting.

When the clock information matches the alarm clock settings based on the match criteria defined by ARM5 - ARM1, the AF (alarm flag) is set. If AFE (alarm flag enable) is also set, the alarm condition activates the $\overline{INT}$ pin 6. To disable the alarm, write “0” to the Date Alarm register and to ARM5 - ARM1.

Note: If the address pointer is allowed to increment to the flag register address, an alarm condition will not cause the interrupt / flag to occur until the address pointer is moved to a different address. It should also be noted that if the last address written is the Second Alarm, the address pointer will increment to the flag address, causing this situation to occur.

The $\overline{INT}$ is cleared by a READ to the Flags register as shown in figure below. A subsequent READ of the Flags register is necessary to see that the value of the alarm flag has been reset to “0”.

Alarm interrupt reset waveform:



Alarm Repeat Mode Settings (addresses 0Bh to 0Eh, ARM5 to ARM1…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Bh	Date Alarm	ARM4	ARM5	20	10	8	4	2	1
0Ch	Hour Alarm	ARM3	0	20	10	8	4	2	1
0Dh	Minute Alarm	ARM2	40	20	10	8	4	2	1
0Eh	Second Alarm	ARM1	40	20	10	8	4	2	1

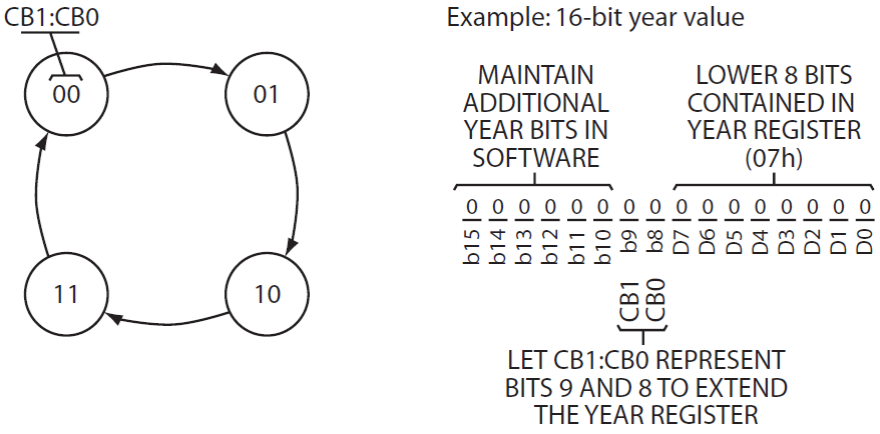
ARM5	ARM4	ARM3	ARM2	ARM1	Alarm setting
1	1	1	1	1	Once per second
1	1	1	1	0	Once per minute
1	1	1	0	0	Once per hour
1	1	0	0	0	Once per day
1	0	0	0	0	Once per month
0	0	0	0	0	Once per year

4.5. CENTURY BITS

The two century bits, CB1 and CB0, are bits 7 and 6, respectively, in the Month / Century register at address 06h. Together, they comprise a 2-bit counter which increments at the turn of each century. CB1 is the most significant bit.

The user may arbitrarily assign the meaning of CB1:CB0 to represent any century value, but the simplest way of using these bits is to extend the Years register (07h) by mapping them directly to bits 9 and 8 (the reader is reminded that the year register is in BCD format). Higher order year bits can be maintained in the application software.

Century bits CB1 and CB0:



4.6. LEAP YEAR

Leap year occurs every four years, in years which are multiples of 4. For example, 2012 was a leap year. An exception to that is any year which is a multiple of 100. For example, the year 2100 is not a leap year. A further exception is that years which are multiples of 400 are indeed leap years. Hence, while 2100 is not a leap year, 2400 is.

During any year which is a multiple of 4, the RV-4162 RTC will automatically insert leap day, February 29. Therefore, the application software must correct for this during the exception years (2100, 2200, etc.) as noted above.

4.7. OSCILLATOR STOP DETECTION

If the oscillator fail (OF) bit is internally set to a “1”, this indicates that the oscillator has either stopped, or was stopped for some period of time and can be used to judge the validity of the clock and date data. This bit will be set to “1” any time the oscillator stops.

In the event the OF bit is found to be set to “1” at any time other than the initial power-up, the STOP bit (OS) should be written to a “1”, then immediately reset to “0”. This will restart the oscillator.

The following conditions can cause the OF bit to be set:

- The first time power is applied (defaults to a “1” on power-up)

  Note: if the OF bit cannot be written to “0” four (4) seconds after the initial power-up, the STOP bit (OS) should be written to a “1”, then immediately reset to “0”.

- The voltage present on V_{DD} or battery is insufficient to support oscillation

- The OS bit is set to “1”

If the oscillator fail interrupt enable bit (OFIE) is set to a “1”, the $\overline{INT}$ pin 6 will also be activated. The $\overline{INT}$ output is cleared by resetting the OFIE or OF bit to “0” (NOT by reading the Flag register).

The OF bit will remain set to “1” until written to logic “0”. The oscillator must start and have run for at least 4 seconds before attempting to reset the OF bit to “0”. If the trigger event occurs during a power-down condition, this bit will be set correctly.

4.8. OUTPUT DRIVER PIN

When the OFIE bit, AFE bit, and Watchdog register are not set to generate an interrupt, the $\overline{INT}$ pin 6 becomes an output driver that reflects the contents of bit 7 (OUT bit) of the Freq. Compensation register. In other words, when bit 7 (OUT bit) is a “0”, then the $\overline{INT}$ pin 6 will be driven low.

Note: The $\overline{INT}$ pin 6 is an open-drain which requires an external pull-up resistor.

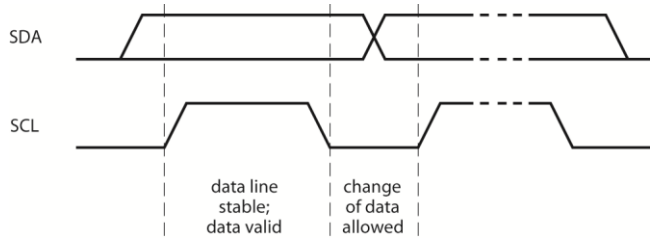
5. CHARACTERISTICS OF THE I²C BUS

The I²C bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial DAta line (SDA) and a Serial CLock line (SCL). Both lines are connected to a positive supply via pull-up resistors. Data transfer is initiated only when the bus is not busy.

5.1. BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line remains stable during the HIGH period of the clock pulse, as changes in the data line at this time are interpreted as a control signals. Data changes should be executed during the LOW period of the clock pulse (see figure below).

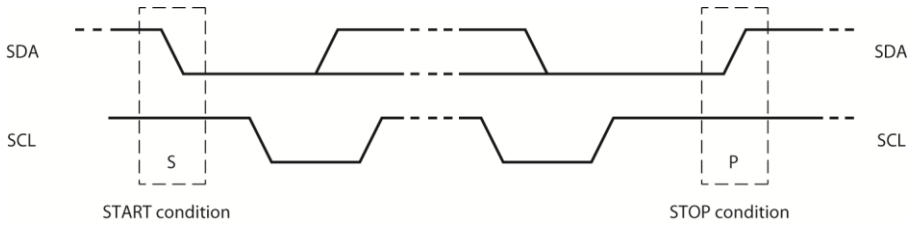
Bit transfer:



5.2. START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the START condition (S). A LOW-to-HIGH transition of the data line, while the clock is HIGH, is defined as the STOP condition (P) (see figure below).

Definition of START and STOP conditions:



For this device, a repeated START is not allowed. Therefore, a STOP has to be released before the next START.

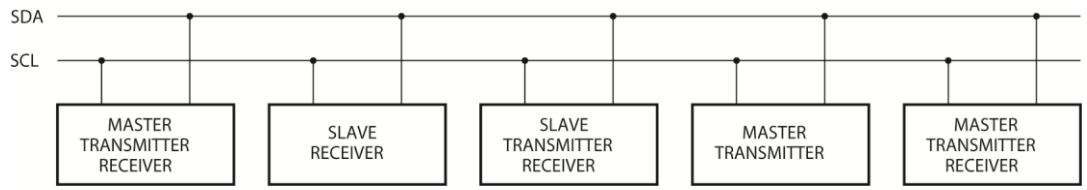
5.3. SYSTEM CONFIGURATION

Since multiple devices can be connected with the I^2C bus, all I^2C bus devices have a fixed and unique device number built-in to allow individual addressing of each device.

The device that controls the I^2C bus is the Master; the devices which are controlled by the Master are the Slaves. A device generating a message is a Transmitter; a device receiving a message is the Receiver. The RV-4162 acts as a Slave-Receiver or Slave-Transmitter.

Before any data is transmitted on the I^2C bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure. The clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line.

System configuration:



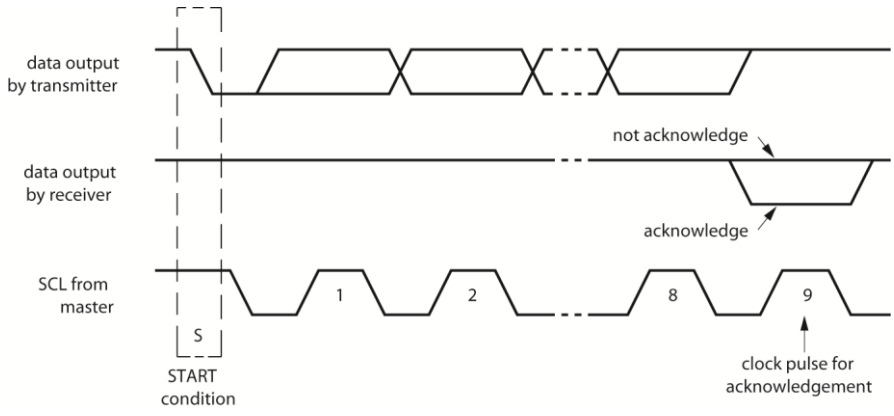
5.4. ACKNOWLEDGE

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of 8 bits is followed by an acknowledge cycle.

- A slave receiver, which is addressed, must generate an acknowledge cycle after the reception of each byte
- Also a master receiver must generate an acknowledge cycle after the reception of each byte that has been clocked out of the slave transmitter
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the related acknowledge clock pulse (set-up and hold times must be considered)
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge cycle on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition

Acknowledgement on the I^2C bus is shown on the figure below.

Acknowledgement on the I^2C bus:



6. I²C BUS PROTOCOL

6.1. ADDRESSING

One I²C bus slave address (1101000) is reserved for the RV-4162. The entire I²C bus slave address byte is shown in the table below:

I²C salve address byte:

Bit	Slave address							
	7 **MSB**	**6**	**5**	**4**	**3**	**2**	**1**	**0** **LSB**
	1	1	0	1	0	0	0	R/$\overline{W}$

After a START condition, the I²C slave address has to be sent to the RV-4162 device.

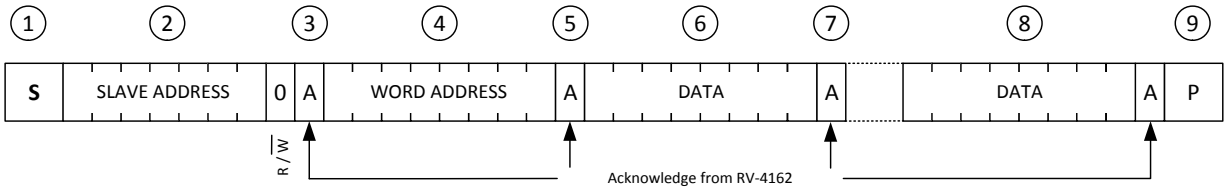
The R/$\overline{W}$ bit defines the direction of the following single or multiple byte data transfer. In the write mode, a data transfer is terminated by sending either the STOP condition or the START condition of the next data transfer.

6.2. CLOCK AND CALENDAR READ AND WRITE CYCLES

6.2.1. WRITE MODE

Master transmits to Slave-Receiver at specified address. The Word Address is 8-bit value that defines which register is to be accessed next. The upper four bits of the Word Address are not used. After reading or writing one byte, the Word Address is automatically incremented by 1.

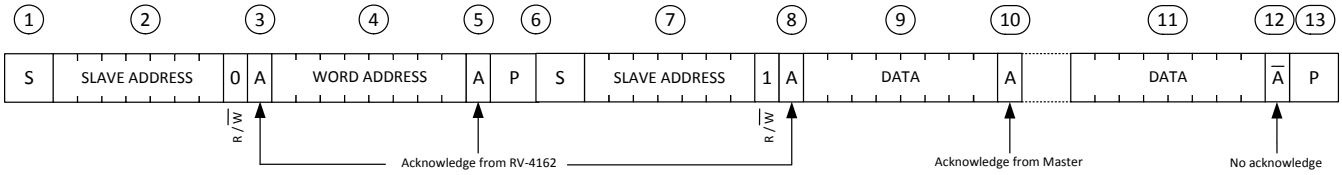
1) Master sends out the “Start Condition”.
2) Master sends out the “Slave Address”, D0h for the RV-4162; the R/$\overline{W}$ bit in write mode.
3) Acknowledgement from the RV-4162.
4) Master sends out the “Word Address” to the RV-4162.
5) Acknowledgement from the RV-4162.
6) Master sends out the “data” to write to the specified address in step 4).
7) Acknowledgement from the RV-4162.
8) Steps 6) and 7) can be repeated if necessary. The address will be incremented automatically in the RV-4162.
9) Master sends out the “Stop Condition”.



6.2.2. READ MODE AT SPECIFIC ADDRESS

Master reads data after setting Word Address:

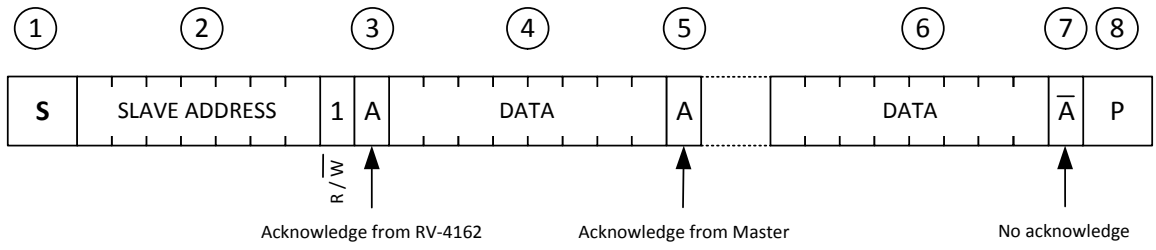
1) Master sends out the “Start Condition”.
2) Master sends out the “Slave Address”, D0h for the RV-4162; the R/$\overline{W}$ bit in write mode.
3) Acknowledgement from the RV-4162.
4) Master sends out the “Word Address” to the RV-4162.
5) Acknowledgement from the RV-4162.
6) Master sends out the “Re-Start Condition” (“Stop Condition” followed by “Start Condition”)
7) Master sends out the “Slave Address”, D1h for the RV-4162; the R/$\overline{W}$ bit in read mode.
8) Acknowledgement from the RV-4162.
   At this point, the Master becomes a Receiver, the Slave becomes the Transmitter.
9) The Slave sends out the “data” from the Word Address specified in step 4).
10) Acknowledgement from the Master.
11) Steps 9) and 10) can be repeated if necessary.
    The address will be incremented automatically in the RV-4162.
12) The Master, addressed as Receiver, can stop data transmission by not generating an acknowledge on the last byte that has been sent from the Slave-Transmitter. In this event, the Slave-Transmitter must leave the data line HIGH to enable the Master to generate a stop condition.
13) Master sends out the “Stop Condition”.



6.2.3. READ MODE

Master reads Slave-Transmitter immediately after first byte:

1) Master sends out the “Start Condition”.
2) Master sends out the “Slave Address”, D1h for the RV-4162; the R/$\overline{W}$ bit in read mode.
3) Acknowledgement from the RV-4162.
   At this point, the Master becomes a Receiver, the Slave becomes the Transmitter
4) The RV-4162 sends out the “data” from the last accessed Word Address incremented by 1.
5) Acknowledgement from the Master.
6) Steps 4) and 5) can be repeated if necessary.
   The address will be incremented automatically in the RV-4162.
7) The Master, addressed as Receiver, can stop data transmission by not generating an acknowledge on the last byte that has been sent from the Slave-Transmitter. In this event, the Slave-Transmitter must leave the data line HIGH to enable the Master to generate a stop condition.
8) Master sends out the “Stop Condition”.



7. ELECTRICAL CHARACTERISTICS

7.1. ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System IEC 60134

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT
Supply voltage	V_{DD}	>GND / <V_{DD}	GND -0.3	+5.0	V
Input voltage	V_I		GND -0.2	V_{DD} +0.3	V
Output voltage	V_O		GND -0.2	V_{DD} +0.3	V
Output current	Io			20	mA
Power dissipation	P_D			1	W
Operating ambient temperature range	T_{OPR}		-40	+85	°C
Storage temperature range	T_{STO}	Stored as bare product	-55	+125	°C
Electro Static Discharge voltage	V_{ESD}	HBM[1] T_A = 25°C MM[2] T_A = 25°C		>1500 >1000	V V

[1] HBM: Human Body Model, according to JESD22-A114.
[2] MM: Machine Model, according to JESD22-A115.

These data are based on characterization results, not tested in production.

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

7.2. OPERATING AND AC MEASUREMENTS CONDITIONS

PARAMETER[1]	RV-4162	UNIT
Supply voltage (V_{DD})	1.3 to 4.4	V
Operating ambient temperature (T_A)	-40 to +85	°C
Load capacitance (C_L)	50	pF
Input rise and fall times	≤5	ns
Input pulse voltages	0.2 V_{DD} to 0.8 V_{DD}	V
Input and output timing ref. voltages	0.3 V_{DD} to 0.7 V_{DD}	V

[1] Output Hi-Z is defined as the point where data is no longer driven.

7.3. CAPACITANCE

PARAMETER[1] [2]	SYMBOL	MIN.	MAX.	UNIT
Input capacitance	C_{IN}	-	7	pF
Output capacitance	C_{OUT}[3]	-	10	pF
Low-pass filter input time constant (SDA and SCL)	t_{LP}	-	50	ns

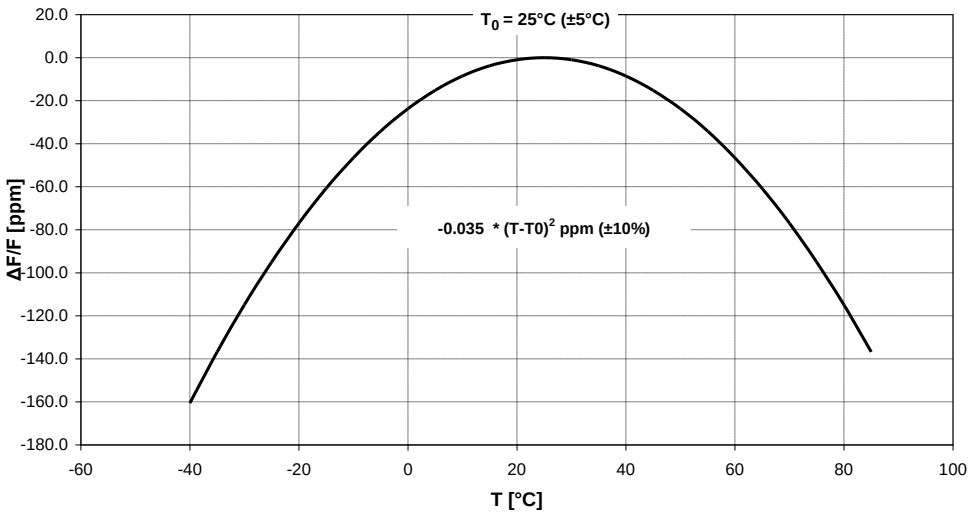
[1] Effective capacitance measured with power supply at 3.6 V; sampled only, not 100% tested.
[2] At 25°C, f = 1 MHz.
[3] Outputs deselected.

7.4. FREQUENCY CHARACTERISTICS

T_{amb}= +25°C; f_{OSC}= 32.768 kHz

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Frequency accuracy	Δf/f	T_{amb} = +25°C			+/-20	ppm
Frequency vs. temperature characteristics	$\Delta f/T_{OPR}$	T_{OPR} = -40°C to +85°C	$-0.035^{ppm}/_{°C^2}(T_{OPR}-T_0)^2$ (+/-10%)			ppm
Turnover temperature	T_O			+25	20 - 30	°C
Aging first year max.	Δf/f	T_{amb} = +25°C			+/-3	ppm
Oscillator start-up voltage	V_{Start}	≤10 seconds	1.5			V
Oscillator start-up time	T_{Start}	V_{DD} = 3.0V			1	s
CLKOUT duty cycle		F_{CLKOUT} = 32.7678 kHz T_{AMB} = +25°C		50	40/60	%

7.5. FREQUENCY VS. TEMPERATURE CHARACTERISTICS



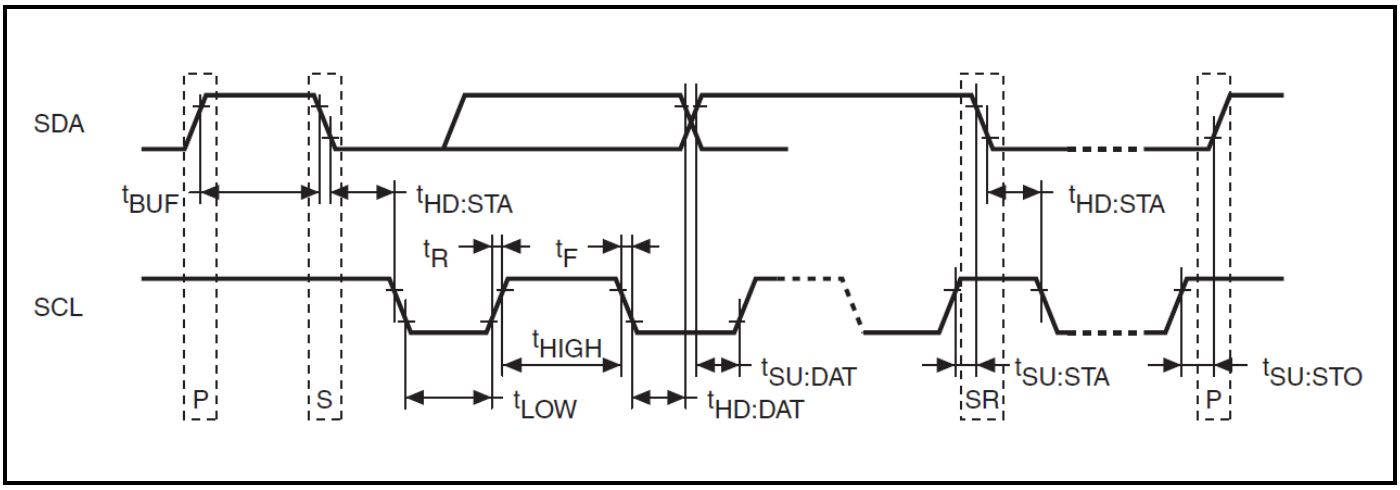
7.6. STATIC CHARACTERISTICS

Valid for T_{amb}= -40°C to +85°C; V_{DD}= 1.3 V to 4.4 V (except where noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{DD} [1)]	Clock	1.0		4.4	V
		I^2C bus (400 kHz)	1.3		4.4	V
Supply current SCL = 400 kHz (no load)	I_{DD1}	V_{DD} = 4.4 V			100	µA
		V_{DD} = 3.6 V		50	70	µA
		V_{DD} = 3.0 V		35		µA
		V_{DD} = 2.5 V		30		µA
		V_{DD} = 2.0 V		20		µA
Supply current (standby) SCL = 0 Hz CLKOUT off All inputs ≥V_{DD} - 0.2 V / ≤V_{SS} + 0.2 V	I_{DD2}	V_{DD} = 4.4 V			950	nA
		V_{DD} = 3.6 V		375	700	nA
		V_{DD} = 3.0 V at 25°C		350	500	nA
		V_{DD} = 2.0 V at 25°C		310	450	nA
		V_{DD} = 1.0 V at 25°C		270	400	nA
LOW level input voltage	V_{IL}		-0.2		0.3 V_{DD}	V
HIGH level input voltage	V_{IH}		0.7 V_{DD}		V_{DD} +0.3	V
HIGH level output voltage	V_{OH}	V_{DD} = 4.4 V I_{OH} = -1.0 mA (push-pull)	2.4			V
LOW level output voltage	V_{OL}	V_{DD} = 4.4 V; I_{OL} = 3.0 mA (SDA)			0.4	V
		V_{DD} = 4.4 V; I_{OL} = 1.0 mA (SQW, $\overline{INT}$)			0.4	
Pull-up supply voltage (open drain)		$\overline{INT}$			4.4	V
Input leakage current	I_{LI}	0 V ≤ V_{IN} ≤ V_{DD}			±1	µA
Output leakage current	I_{LO}	0 V ≤ V_{OUT} ≤ V_{DD}			±1	µA

[1)] Oscillator start-up guaranteed at 1.5 V only.

7.7. I²C INTERFACE TIMING CHARACTERISTICS



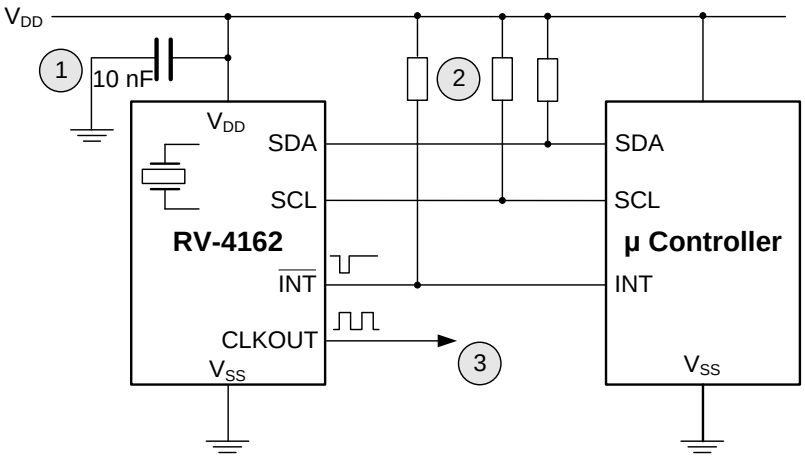
Valid for T_{amb} = -40°C to +85°C; V_{DD}= 1.3 V to 4.4 V (except where noted)

PARAMETER	SYMBOL		MIN	MAX	UNIT
SCL Clock Frequency	f_{SCL}		0	400	kHz
Start Condition Set-up Time (only relevant for a repeated start condition)	$t_{SU;STA}$		600		ns
Start Condition Hold Time (after this period the first clock pulse is generated)	$t_{HD;STA}$		600		ns
Data Set-up Time[1)]	$t_{SU;DAT}$		100		ns
Data Hold Time	$t_{HD;DAT}$		0		µs
Stop Condition Set-up Time	$t_{SU;STO}$		600		ns
Bus Free Time between STOP and START condition	t_{BUF}		1.3		µs
SCL “LOW time”	t_{LOW}		1.3		µs
SCL “HIGH time”	t_{HIGH}		600		ns
SCL and SDA Rise Time	t_r			300	ns
SCL and SDA Fall Time	t_f			300	ns
Watchdog Output Pulse Width	t_{rec}		96	98	ms

[1)] Transmitter must internally provide a hold time to bridge the undefined region (300 ns max) of the falling edge of SCL.

8. APPLICATION INFORMATION

Operating RV-4162:

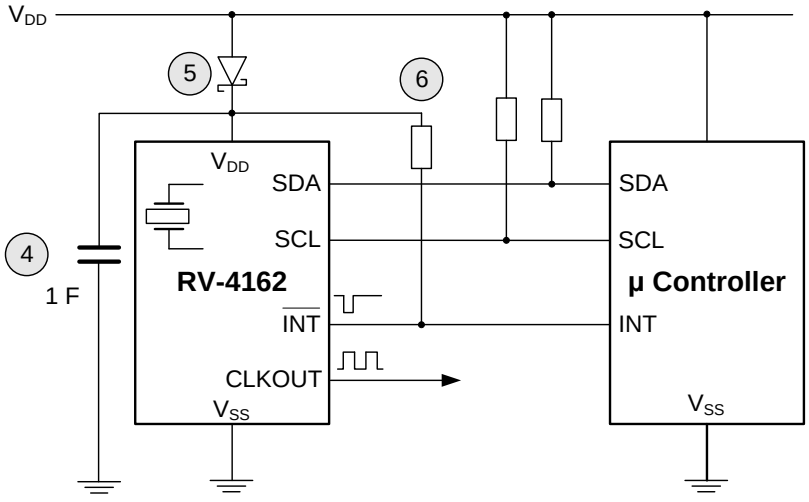


1 A 10 nF decoupling capacitor is recommended close to the device.

2 Interface lines SCL, SDA and $\overline{INT}$ are open drain and require pull-up resistor to $V_{DD.}$

3 CLKOUT offers selectable frequencies 1 Hz to 32.768 kHz for application use. If not used, it is recommended to disable CLKOUT for optimized current consumption.

Operating RV-4162 with SuperCap backup supply voltage:



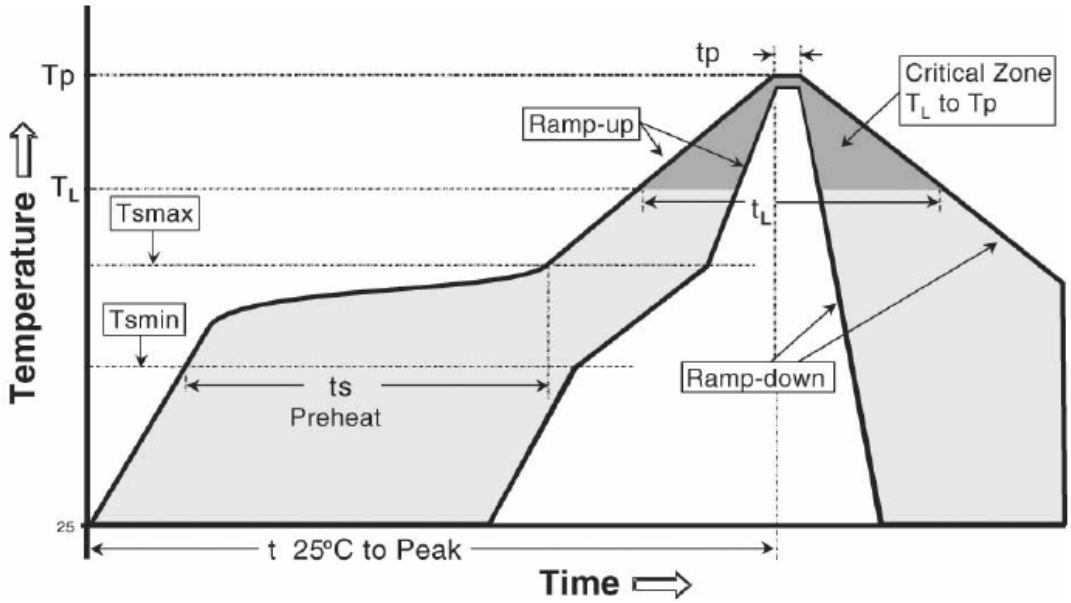
4 A SuperCap combined with a low Vf diode can be used to operate the RV-4162 in stand-by or backup supply voltage mode.

5 If a SuperCap is used, it is recommended using a Schottky diode due to its low forward voltage Vf.

6 If application requires, the $\overline{INT}$ pull-up resistor can be tied to the backup supply voltage, in order to generate an interrupt even when main supply voltage V_{DD} is off.

8.1. RECOMMENDED REFLOW TEMPERATURE (LEADFREE SOLDERING)

Maximum Reflow Conditions in accordance with IPC/JEDEC J-STD-020C "Pb-free"



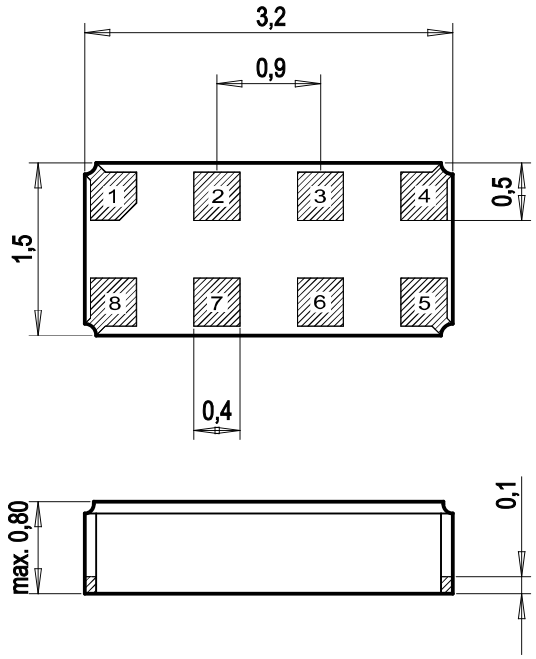
Temperature Profile	Symbol	Condition	Unit
Average ramp-up rate	(Ts_{max} to Tp)	3°C / second max	°C / s
Ramp down Rate	T_{cool}	6°C / second max	°C / s
Time 25°C to Peak Temperature	$T_{to\text{-}peak}$	8 minutes max	m
Preheat			
Temperature min	Ts_{min}	150	°C
Temperature max	Ts_{max}	200	°C
Time Ts_{min} to Ts_{max}	ts	60 - 180	Sec
Soldering above liquidus			
Temperature liquidus	T_L	217	°C
Time above liquidus	t_L	60 – 150	sec
Peak temperature			
Peak Temperature	Tp	260	°C
Time within 5°C of peak temperature	tp	20 - 40	sec

9. PACKAGES

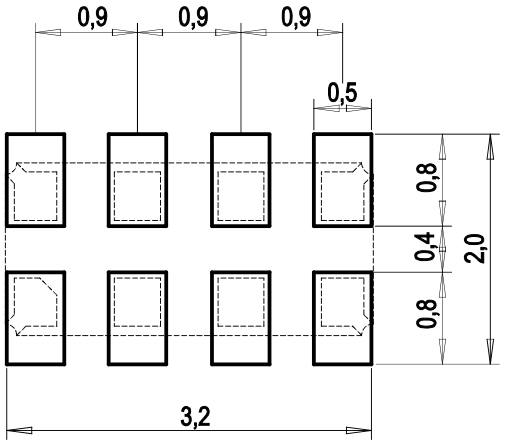
9.1. DIMENSIONS AND SOLDERPADS LAYOUT

C7 Package:

Package dimensions (bottom view):



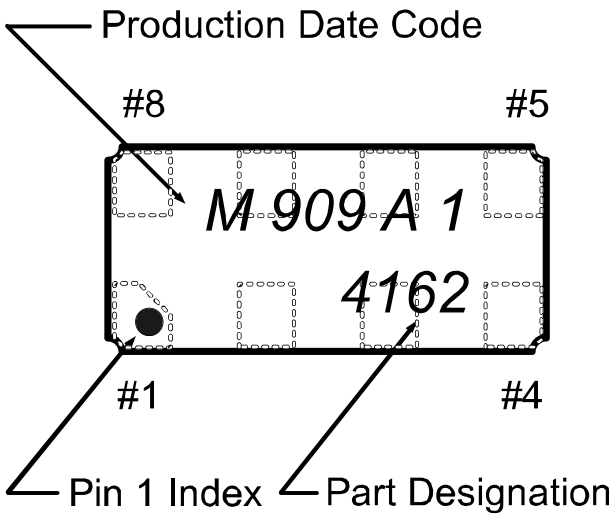
Recommended solderpad layout:



All dimensions in mm typical.

9.2. MARKING AND PIN #1 INDEX

C7 Package:

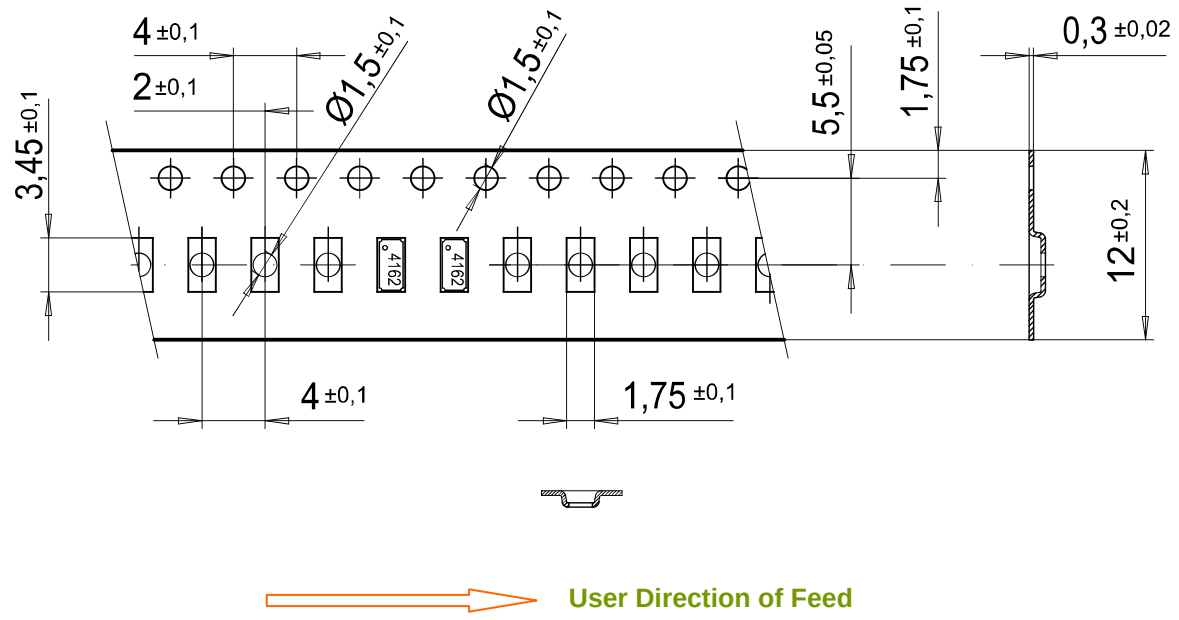


10.PACKING INFORAMTION

10.1. CARRIER TAPE

12 mm Carrier-Tape:	Material:	Polystyrene / Butadine or Polystyrol black, conductive
Cover Tape:	Base Material:	Polyester, conductive 0.061 mm
	Adhesive Material:	Pressure-sensitive Synthetic Polymer
	Peel Method:	Middle part removed, sticky sides remain on carrier

C7 Package:



Tape Leader and Trailer: 300 mm minimum.
All dimensions in mm.

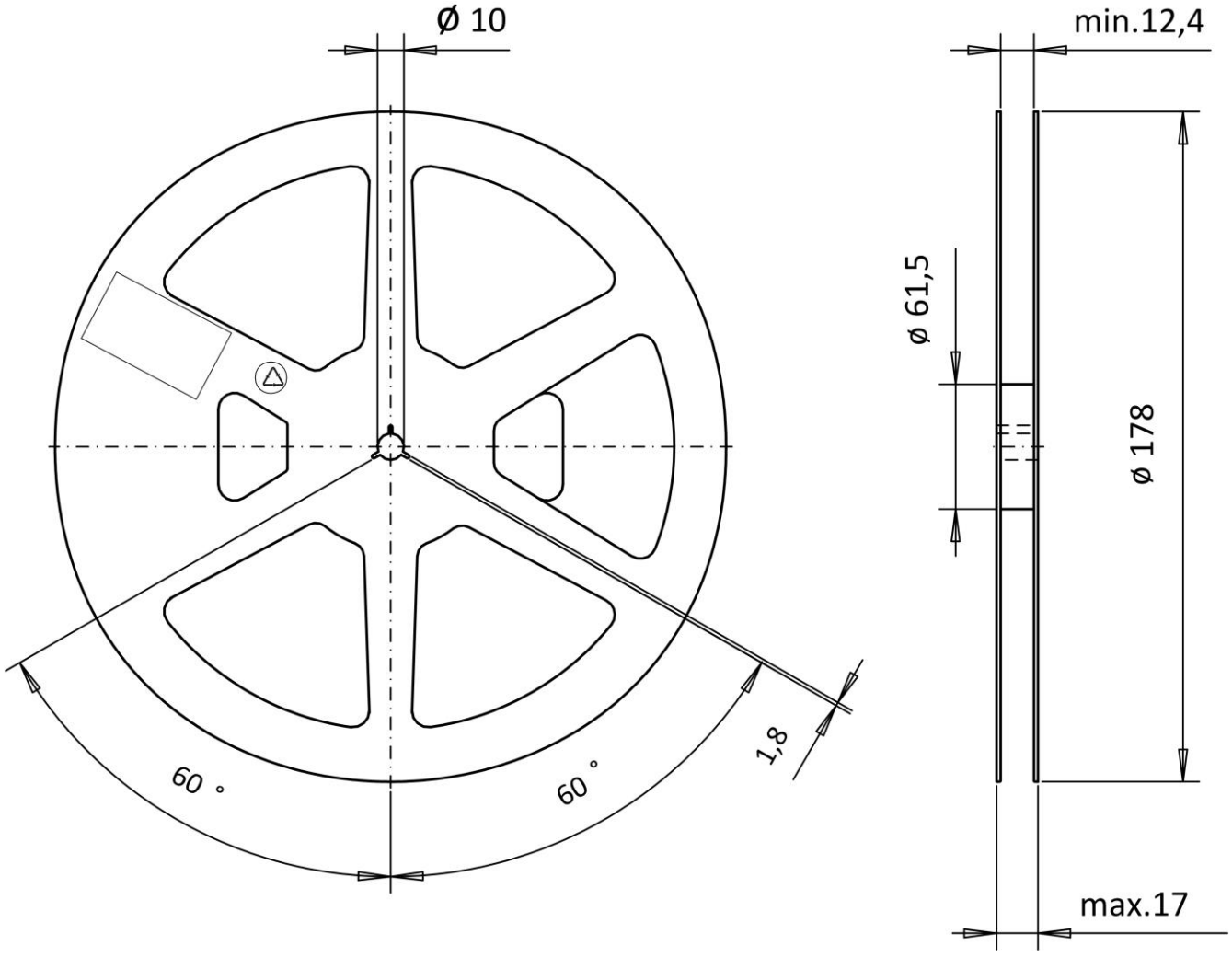
10.2. PARTS PER REEL

C7 Package:

Reels:

Diameter	Material	RTC's per reel
7"	Plastic, Polystyrol	1'000
7"	Plastic, Polystyrol	5'000

10.3. REEL 7 INCH FOR 12 mm TAPE



Reel:

Diameter	Material
7"	Plastic, Polystyrol

10.4. HANDLING PRECAUTIONS FOR CRYSTALS OR MODULES WITH EMBEDDED CRYSTALS

The built-in tuning-fork crystal consists of pure Silicon Dioxide in crystalline form. The cavity inside the package is evacuated and hermetically sealed in order for the crystal blank to function undisturbed from air molecules, humidity and other influences.

Shock and vibration:

Keep the crystal / module from being exposed to **excessive mechanical shock and vibration**. Micro Crystal guarantees that the crystal / module will bear a mechanical shock of 5000g / 0.3 ms.

The following special situations may generate either shock or vibration:

Multiple PCB panels - Usually at the end of the pick & place process the single PCBs are cut out with a router. These machines sometimes generate vibrations on the PCB that have a fundamental or harmonic frequency close to 32.768 kHz. This might cause breakage of crystal blanks due to resonance. Router speed should be adjusted to avoid resonant vibration.

Ultrasonic cleaning - Avoid cleaning processes using ultrasonic energy. These processes can damages crystals due to mechanical resonance of the crystal blank.

Overheating, rework high temperature exposure:

Avoid overheating the package. The package is sealed with a seal ring consisting of 80% Gold and 20% Tin. The eutectic melting temperature of this alloy is at 280°C. Heating the seal ring up to >280°C will cause melting of the metal seal which then, due to the vacuum, is sucked into the cavity forming an air duct. This happens when using hot-air-gun set at temperatures >300°C.

Use the following methods for rework:

- Use a hot-air- gun set at 270°C.
- Use 2 temperature controlled soldering irons, set at 270°C, with special-tips to contact all solder-joints from both sides of the package at the same time, remove part with tweezers when pad solder is liquid.

11.DOCUMENT REVISION HISTORY

Date	Revision #	Revision Details
April 2010	1.2	First release
December 2013	2.0	New version
January 2014	2.1	Static characteristics corrections