Application Manual

RV-8263-C8

Ultra-Small Real-Time Clock Module with I²C-Bus Interface

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Ultra Small Real-Time Clock Module with I²C-Bus Interface

1. OVERVIEW

- RTC module with built-in “Tuning Fork” crystal oscillating at 32.768 kHz
- Counters for seconds, minutes, hours, date, weekday, month and year
- Programmable Offset register for frequency adjustment
- Automatic leap year calculation (2000 to 2099)
- Alarm Interrupts for second, minutes, hour, date and weekday settings
- Countdown Timer Interrupt function
- Minute and Half Minute Interrupt
- Oscillator stop detection function
- Internal Power-On Reset (POR)
- Programmable Clock Output for peripheral devices (32.768 kHz, 16.384 kHz, 8.192 kHz, 4.096 kHz, 2.048 kHz, 1.024 kHz and 1 Hz) with enable/disable function (CLKOE)
- I²C-bus interface (up to 400 kHz)
- Wide operating voltage range: 0.9 V to 5.5 V
- Wide interface operating voltage: 1.8 to 5.5 V
- Very low current consumption: 190 nA (V_{DD} = 3.0 V, T_A = 25°C)
- Operating temperature range: -40 to +85°C
- Ultra-miniature ceramic SMD package with metal lid, RoHS-compliant and 100% lead-free: 2.0 x 1.2 x 0.70 mm
- Ultra-low profile (maximum height 0.70 mm), lightweight (5.1 mg)
- Automotive qualification according to AEC-Q200 available

1.1. GENERAL DESCRIPTION

The RV-8263-C8 is a CMOS real-time clock/calendar module optimized for low power consumption. An Offset register makes it possible to compensate for the frequency deviation of the clock of 32.768 kHz. All addresses and data are transferred over an I²C-bus interface for communication with a host controller. The register address is incremented automatically after each written or read data byte.
This ultra-small and lightweight RTC module has been specially designed for miniature and cost sensitive high volume applications.

1.2. APPLICATIONS

The RV-8263-C8 RTC module combines standard RTC functions in high reliable, ultra-small ceramic package:

- Smallest RTC module (embedded XTAL) in miniature 2.0 x 1.2 x 0.70 mm lead-free ceramic package
- Price competitive

The unique size and the competitive pricing make this product perfectly suitable for many applications where high circuit density or a smaller PCB is required:

- Communication: IoT / Wearables / Wireless Sensors and Tags / Handsets
- Automotive: M2M / Navigation & Tracking Systems / Dashboard / Tachometers / Engine Controller Car Audio & Entertainment Systems
- Metering: E-Meter / Heating Counter / Smart Meters / PV Converter
- Outdoor: ATM & POS systems / Surveillance & Safety systems / Ticketing Systems
- Medical: Glucose Meter / Health Monitoring Systems
- Safety: Security & Camera Systems / Door Lock & Access Control
- Consumer: Gambling Machines / TV & Set Top Boxes / White Goods
- Automation: PLC / Data Logger / Home & Factory Automation / Industrial and Consumer Electronics

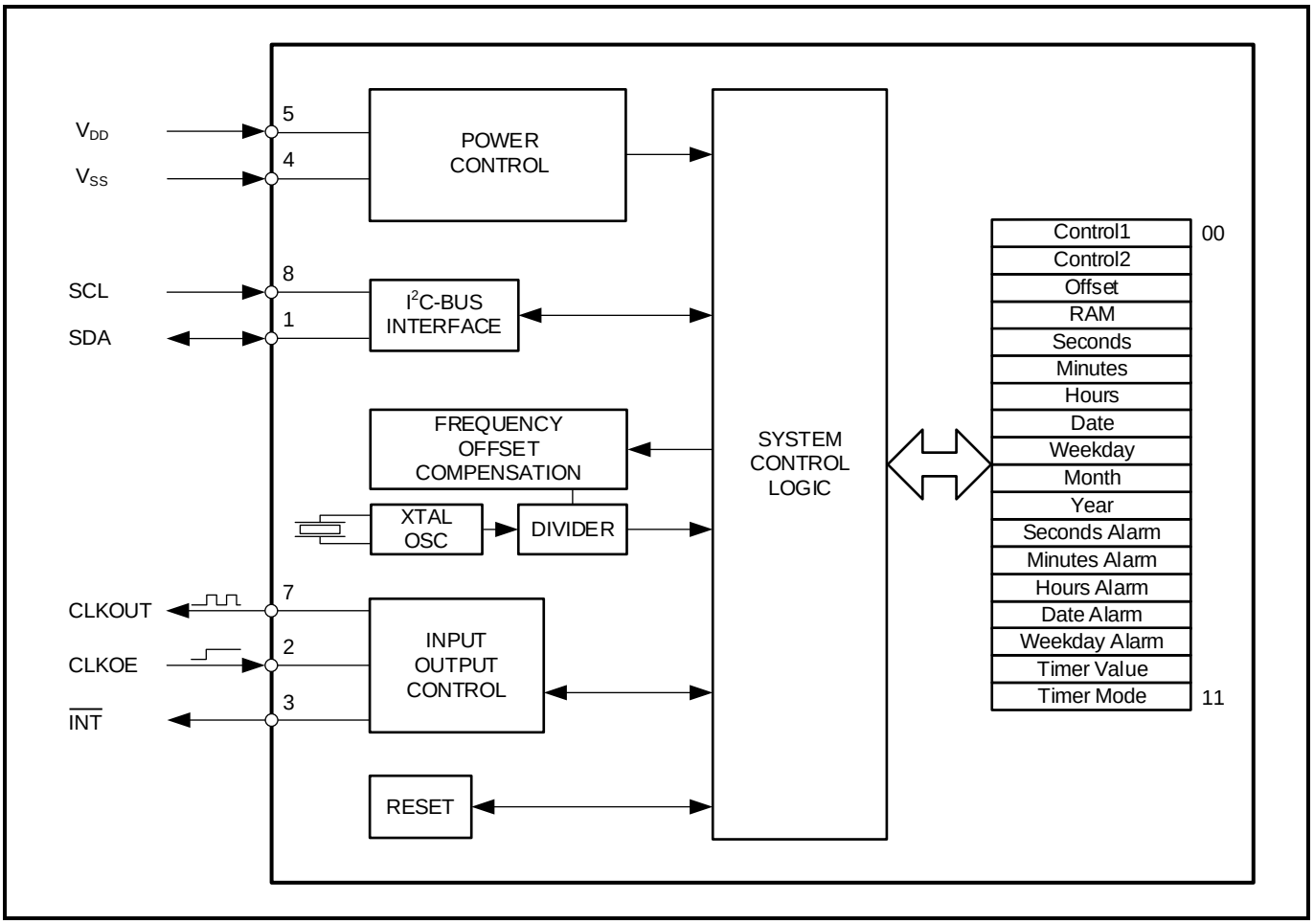
1.3. ORDERING INFORMATION

Example: RV-8263-C8 TA QC

Code	Operating temperature range
TA (Standard)	-40 to +85°C

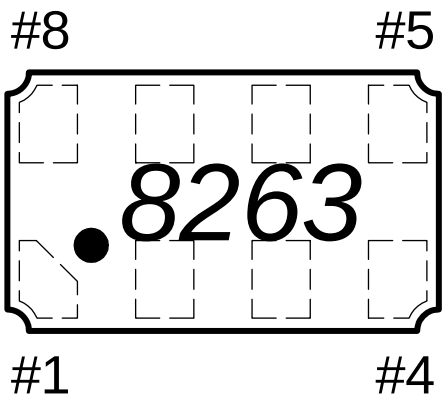
Code	Qualification
QC (Standard)	Commercial Grade
QA	Automotive Grade AEC-Q200

2. BLOCK DIAGRAM



2.1. PINOUT

RV-8263-C8 Package: (top view)



#1	SDA
#2	CLKOE
#3	$\overline{INT}$
#4	V_{SS}
#5	V_{DD}
#6	NC
#7	CLKOUT
#8	SCL

2.2. PIN DESCRIPTION

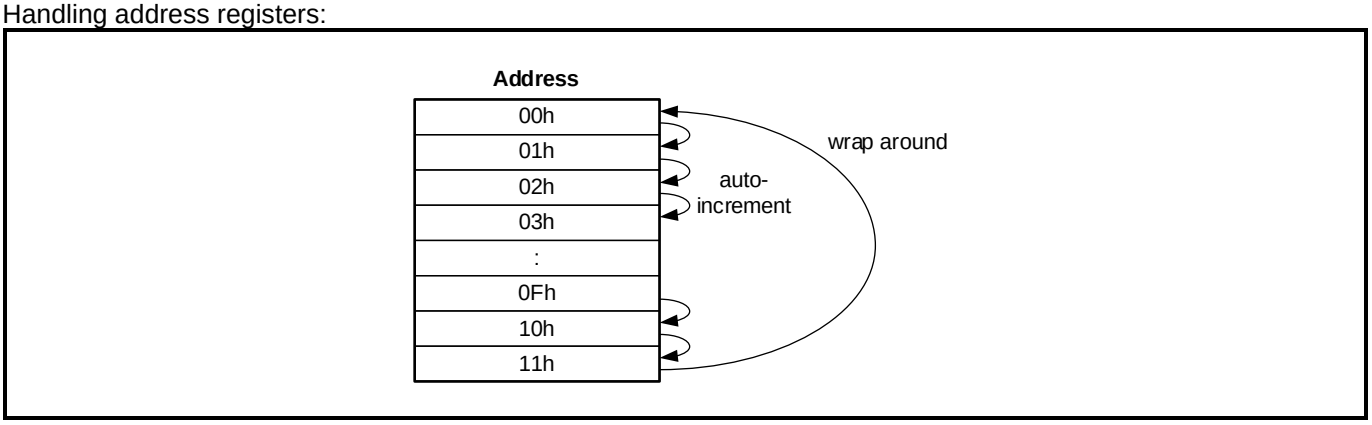
Symbol	Pin #	Description
SDA	1	I²C Serial Data Input-Output; open-drain; requires pull-up resistor.
CLKOE	2	Input to enable the CLKOUT pin. If CLKOE is HIGH, the CLKOUT pin is in output mode. When CLKOE is tied to Ground, the CLKOUT pin is LOW.
$\overline{INT}$	3	Interrupt Output; open-drain; active LOW; requires pull-up resistor; Used to output alarm, minute, half minute, countdown timer and compensation Interrupt signals.
V_{SS}	4	Ground.
V_{DD}	5	Power Supply Voltage.
NC	6	Not connected. Is internally connected and should be left floating.
CLKOUT	7	Clock Output; push-pull; controlled by CLKOE. If CLKOE is HIGH (V_{DD}), the CLKOUT pin drives the square wave of 32.768 kHz, 16.384 kHz, 8.192 kHz, 4.096 kHz, 2.048 kHz, 1.024 kHz or 1 Hz (Default value is 32.768 kHz). When CLKOE is tied to Ground, the CLKOUT pin is LOW.
SCL	8	I²C Serial Clock Input; requires pull-up resistor.

2.3. FUNCTIONAL DESCRIPTION

The RV-8263-C8 is a low power CMOS real-time clock/calendar module with embedded 32.768 kHz Crystal. The CMOS IC contains 18 8-bit registers with an auto-incrementing register address, a frequency divider which provides the source clock for the Real Time Clock (RTC), a programmable clock output, and an I²C-Bus interface (2 wires). The Offset register allows to digitally adjust the 32.768 kHz oscillator frequency in order to compensate and minimize time deviation.

The built-in address register will increment automatically after each read or write of a data byte up to the register 11h. After register 11h, the auto-incrementing will wrap around to address 00h (see following Figure).

Handling address registers:

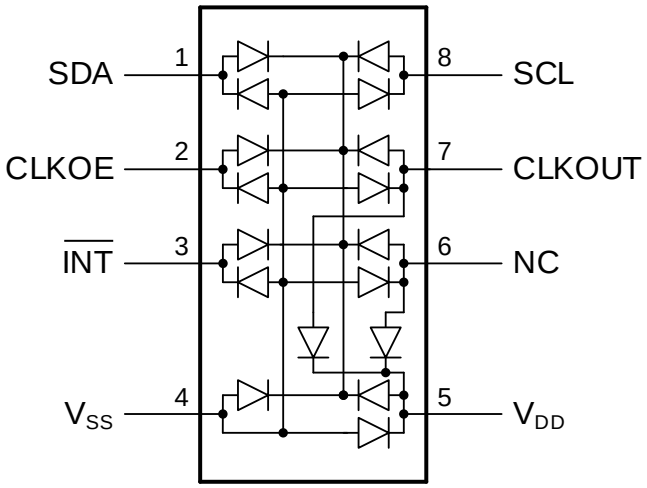


All registers (see REGISTER OVERVIEW) are designed as addressable 8-bit parallel registers although not all bits are implemented.

- The first two registers (memory address 00h and 01h) are used as control and status register.
- The register at address 02h is an Offset register allowing the compensation of time deviation.
- The register at address 03h is a free User RAM byte.
- The addresses 04h through 0Ah are used as counters for the clock function (seconds up to year counters).
- Address locations 0Bh through 0Fh contain alarm registers which define the conditions for an alarm.
- The registers at 10h and 11h are for the timer function.

The Seconds, Minutes, Hours, Date, Month and Year as well as the corresponding alarm registers are all coded in Binary Coded Decimal (BCD) format. When one of the RTC registers is written or read, the contents of all time counters are frozen. Therefore, faulty writing or reading of the clock and calendar during a carry condition is prevented for up to 1 second.

2.4. DEVICE PROTECTION DIAGRAM



3. REGISTER ORGANIZATION

Registers are accessed by selecting a register address and then performing read or write operations. Multiple reads or writes may be executed in a single access, with the address automatically incrementing after each byte.
18 registers (00h – 11h) are available. The time registers are encoded in the Binary Coded Decimal format (BCD) to simplify application use. Other registers are either bit-wise or standard binary format. When one of the RTC registers is written or read, the contents of all time counters are frozen for up to 1 second. Therefore, faulty writing or reading of the clock and calendar during a carry condition is prevented.

3.1. REGISTER OVERVIEW

After reset, all registers are set according to Table in section REGISTER RESET VALUES SUMMARY.

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	Control1	TEST	SR	STOP	SR		CIE	12_24	CAP
01h	Control2	AIE	AF	MI	HMI	TF	FD		
02h	Offset	MODE	OFFSET						
03h	RAM	RAM data							
04h	Seconds	OS	40	20	10	8	4	2	1
05h	Minutes	X	40	20	10	8	4	2	1
06h	Hours (24 hour)	X	X	20	10	8	4	2	1
	Hours (12 hour)			AMPM	10	8	4	2	1
07h	Date	X	X	20	10	8	4	2	1
08h	Weekday	X	X	X	X	X	4	2	1
09h	Month	X	X	X	10	8	4	2	1
0Ah	Year	80	40	20	10	8	4	2	1
0Bh	Seconds Alarm	AE_S	40	20	10	8	4	2	1
0Ch	Minutes Alarm	AE_M	40	20	10	8	4	2	1
0Dh	Hours Alarm (24h)	AE_H	X	20	10	8	4	2	1
	Hours Alarm (12h)			AMPM	10	8	4	2	1
0Eh	Date Alarm	AE_D	X	20	10	8	4	2	1
0Fh	Weekday Alarm	AE_W	X	X	X	X	4	2	1
10h	Timer Value	128	64	32	16	8	4	2	1
11h	Timer Mode	X	X	X	TD		TE	TIE	TI_TP
Bit positions labeled as X are not implemented and will return a 0 when read.									

3.2. CONTROL REGISTERS

To ensure that all control registers will be set to their default values, the V_{DD} level must be at zero volts at initial power-up. If this is not possible, a reset must be initiated with the software reset command when power is stable. Refer to section SOFTWARE RESET for details.

00h - Control1

Control and status register 1.

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	Control1	TEST	SR	STOP	SR		CIE	12_24	CAP
	Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Value	Description
7	TEST	0	Normal mode.
		1	External clock test mode. Do not use.
6	SR	Software Reset (see SOFTWARE RESET)	
		0	No software reset.
		1	Initiate software reset; this bit always returns a 0 when read. For a software reset, 01011000 (58h) must be sent to register Control1.
5	STOP	STOP bit (see STOP BIT FUNCTION)	
		0	RTC clock runs.
		1	RTC clock is stopped; the upper part of the RTC divider chain flip-flops (prescaler F2 to F14) are asynchronously set logic 0. The CLKOUT frequencies 32.768 kHz, 16.384 kHz and 8.192 kHz are still available.
4:3	SR	Software Reset (see SOFTWARE RESET)	
		00	No software reset.
		11	Initiate software reset; this bits always returns a 0 when read. For a software reset, 01011000 (58h) must be sent to register Control1.
2	CIE	Compensation Interrupt Enable (see FREQUENCY OFFSET COMPENSATION)	
		0	No compensation interrupt will be generated.
		1	Compensation interrupt pulses will be generated on pin $\overline{INT}$ at every compensation cycle.
1	12_24	12 or 24 hour mode (see TIME AND DATE REGISTERS and ALARM REGISTERS)	
		0	24 hour mode is selected (0 to 23).
		1	12 hour mode is selected (1 to 12).
0	CAP	0	Must always be written with logic 0.

01h - Control2

Control and status register 2.

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01h	Control2	AIE	AF	MI	HMI	TF	FD		
	Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Value	Description
7	AIE	Alarm Interrupt Enable (see ALARM FUNCTION and INTERRUPT OUTPUT)	
		0	Disabled
		1	Enabled
6	AF	Alarm Flag (see ALARM FUNCTION and INTERRUPT OUTPUT)	
		0	Read: Alarm Flag inactive Write: Alarm Flag is cleared
		1	Read: Alarm Flag active Write: Alarm Flag remains unchanged
5	MI	Minute Interrupt Enable (see MINUTE AND HALF MINUTE INTERRUPT FUNCTION and TIMER FLAG TF)	
		0	Disabled
		1	Enabled
4	HMI	Half Minute Interrupt Enable (see MINUTE AND HALF MINUTE INTERRUPT FUNCTION and TIMER FLAG TF)	
		0	Disabled
		1	Enabled
3	TF	Timer Flag (see COUNTDOWN TIMER FUNCTION, INTERRUPT OUTPUT and TIMER FLAG TF)	
		0	No timer interrupt generated
		1	Flag set when timer interrupt generated
2:0	FD	000 to 111	CLKOUT Frequency (see CLKOUT FREQUENCY SELECTION)

FD	CLKOUT Frequency
000	32.768 kHz – Default value
001	16.384 kHz
010	8.192 kHz
011	4.096 kHz
100	2.048 kHz
101	1.024 kHz
110	1 Hz (1)
111	CLKOUT = LOW

(1) 1 Hz clock pulses are affected by compensation pulses (see FREQUENCY OFFSET COMPENSATION).

02h – Offset Register

This register holds the OFFSET value to digitally compensate the initial frequency deviation of the 32.768 kHz oscillator or for aging adjustment (see FREQUENCY OFFSET COMPENSATION).

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
02h	Offset	MODE	OFFSET						
	Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Value	Description
7	MODE		Offset Mode
		0	Normal Mode: Offset is made once every two hours.
		1	Fast Mode: Offset is made every 4 minutes.
6:0	OFFSET	-64 to +63	Offset value. For MODE = 0, each LSB introduces an offset of 4.34 ppm. For MODE = 1, each LSB introduces an offset of 4.069 ppm. The values of 4.34 ppm and 4.069 ppm are based on a nominal 32.768 kHz clock. The offset value is coded in two's complement giving a range of +63 LSB to -64 LSB (see FREQUENCY OFFSET COMPENSATION).

OFFSET	OFFSET compensation value in decimal	Compensation pulses in steps	CLKOUT frequency offset in ppm(1)	
			Normal Mode MODE = 0	Fast Mode MODE = 1
0111111	63	+63	+273.420	+256.347
0111110	62	+62	+269.080	+252.278
:	:	:	:	:
0000001	1	+1	+4.340	+4.069
0000000	0	0	0	0
1111111	127	-1	-4.340	-4.069
1111110	126	-2	-8.680	-8.138
:	:	:	:	:
1000001	65	-63	-273.420	-256.347
1000000	64	-64	-277.760	-260.416

(1) The frequency offset measured at CLKOUT pin can be compensated by computing the compensation value OFFSET and writing it into the Offset register (see OFFSET COMPENSATION CALCULATION WORKFLOW).

03h - RAM

Free RAM byte, which can be used for any purpose, for example, status byte of the system.

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
03h	RAM	RAM data							
	Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Value	Description
7:0	RAM	00h to FFh	User RAM

3.3. TIME AND DATE REGISTERS

04h - Seconds

This register holds the count of seconds, in two binary coded decimal (BCD) digits. Values will be from 00 to 59.

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
04h	Seconds	OS	40	20	10	8	4	2	1
	Reset	1	0	0	0	0	0	0	0

Bit	Symbol	Value	Description
7	OS		Oscillator Stop (see OSCILLATOR STOP FLAG)
		0	Clock integrity is guaranteed.
		1	Clock integrity is not guaranteed; oscillator has stopped or has been interrupted. – Default value
6:0	Seconds	00 to 59	Holds the count of seconds, coded in BCD format.

05h - Minutes

This register holds the count of minutes, in two binary coded decimal (BCD) digits. Values will be from 00 to 59.

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
05h	Minutes	X	40	20	10	8	4	2	1
	Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Value	Description
7	X	0	Unused
6:0	Minutes	00 to 59	Holds the count of minutes, coded in BCD format.

06h – Hours

This register holds the count of hours, in two binary coded decimal (BCD) digits. If the 12_24 bit is cleared (default) (see CONTROL REGISTERS, 00h - Control1) the values will be from 0 to 23. If the 12_24 bit is set, the hour values will range from 1 to 12 and the AMPM bit will be 0 for AM hours and 1 for PM hours.

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
06h	Hours (24 hour mode) – default value	X	X	20	10	8	4	2	1
	Hours (12 hour mode)			AMPM	10	8	4	2	1
	Reset	0	0	0	0	0	0	0	0

Hours (24 hour mode), 12_24 = 0 – default value

Bit	Symbol	Value	Description
7:6	X	0	Unused
5:0	Hours (24 hour mode) – default value	0 to 23	Holds the count of hours, coded in BCD format.

Hours (12 hour mode), 12_24 = 1

Bit	Symbol	Value	Description
7:6	X	0	Unused
5	AMPM	0	AM hours.
		1	PM hours.
4:0	Hours (12 hour mode)	1 to 12	Holds the count of hours, coded in BCD format.

07h – Date

This register holds the current date of the month, in two binary coded decimal (BCD) digits. Values will range from 01 to 31. Leap years are correctly handled from 2000 to 2099.

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
07h	Date	X	X	20	10	8	4	2	1
	Reset	0	0	0	0	0	0	0	1

Bit	Symbol	Value	Description
7:6	X	0	Unused
5:0	Date	01 to 31	Holds the current date of the month, coded in BCD format. – Default value = 01

08h - Weekday

This register holds the current day of the week. Each value represents one weekday that is assigned by the user. Values will range from 0 to 6.

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08h	Weekday	X	X	X	X	X	4	2	1
	Reset	0	0	0	0	0	1	1	0

Bit	Symbol	Value	Description
7:3	X	0	Unused
2:0	Weekday	0 to 6	Holds the weekday counter value.

Weekday	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Weekday 1	0	0	0	0	0	0	0	0
Weekday 2						0	0	1
Weekday 3						0	1	0
Weekday 4						0	1	1
Weekday 5						1	0	0
Weekday 6						1	0	1
Weekday 7 – Default value						1	1	0

09h - Month

This register holds the current month, in two binary coded decimal (BCD) digits. Values will range from 01 to 12.

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
09h	Month	X	X	X	10	8	4	2	1
	Reset	0	0	0	0	0	0	0	1

Bit	Symbol	Value	Description
7:5	X	0	Unused
4:0	Month	01 to 12	Holds the current month, coded in BCD format.

Month	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
January – Default value	0	0	0	0	0	0	0	1
February				0	0	0	1	0
March				0	0	0	1	1
April				0	0	1	0	0
May				0	0	1	0	1
June				0	0	1	1	0
July				0	0	1	1	1
August				0	1	0	0	0
September				0	1	0	0	1
October				1	0	0	0	0
November				1	0	0	0	1
December				1	0	0	1	0

0Ah - Year

This register holds the current year, in two binary coded decimal (BCD) digits. Values will range from 00 to 99. Leap years are correctly handled from 2000 to 2099.

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Ah	Year	80	40	20	10	8	4	2	1
	Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Value	Description
7:0	Year	00 to 99	Holds the current year, coded in BCD format.

3.4. ALARM REGISTERS

0Bh – Seconds Alarm

This register holds the Seconds Alarm Enable bit AE_S and the alarm value for seconds, in two binary coded decimal (BCD) digits. Values will range from 00 to 59.

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Bh	Seconds Alarm	AE_S	40	20	10	8	4	2	1
	Reset	1	0	0	0	0	0	0	0

Bit	Symbol	Value	Description
7	AE_S		Seconds Alarm Enable bit (see ALARM FUNCTION)
		0	Enabled
		1	Disabled – Default value
6:0	Seconds Alarm	00 to 59	Holds the alarm value for seconds, coded in BCD format.

0Ch – Minutes Alarm

This register holds the Minutes Alarm Enable bit AE_M and the alarm value for minutes, in two binary coded decimal (BCD) digits. Values will range from 00 to 59.

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Ch	Minutes Alarm	AE_M	40	20	10	8	4	2	1
	Reset	1	0	0	0	0	0	0	0

Bit	Symbol	Value	Description
7	AE_M		Minutes Alarm Enable bit (see ALARM FUNCTION)
		0	Enabled
		1	Disabled – Default value
6:0	Minutes Alarm	00 to 59	Holds the alarm value for minutes, coded in BCD format.

0Dh – Hours Alarm

This register holds the Hours Alarm Enable bit AE_H and the alarm value for hours, in two binary coded decimal (BCD) digits. If the 12_24 bit is cleared (default value) (see CONTROL REGISTERS, 00h - Control1) the values will range from 00 to 23. If the 12_24 bit is set, the hour values will be from 01 to 12 and the AMPM bit will be 0 for AM hours and 1 for PM hours.

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Dh	Hours Alarm (24 hour mode) – default value	AE_H	X	20	10	8	4	2	1
	Hours Alarm (12 hour mode)			AMPM	10	8	4	2	1
	Reset	1	0	0	0	0	0	0	0

Hours Alarm (24 hour mode), 12_24 = 0 – default value

Bit	Symbol	Value	Description
7	AE_H		Hours Alarm Enable bit (see ALARM FUNCTION)
		0	Enabled
		1	Disabled – Default value
6	X	0	Unused
5:0	Hours Alarm (24 hour mode) – default value	00 to 23	Holds the alarm value for hours, coded in BCD format.

Hours Alarm (12 hour mode), 12_24 = 1

Bit	Symbol	Value	Description
7	AE_H		Hours Alarm Enable bit (see ALARM FUNCTION)
		0	Enabled
		1	Disabled – Default value
6	X	0	Unused
5	AMPM	0	AM hours.
		1	PM hours.
4:0	Hours Alarm (12 hour mode)	01 to 12	Holds the alarm value for hours, coded in BCD format.

0Eh - Date Alarm

This register holds the Date Alarm Enable bit AE_D and the alarm value for the date, in two binary coded decimal (BCD) digits. Values will range from 01 to 31.

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Eh	Date Alarm	AE_D	X	20	10	8	4	2	1
	Reset	1	0	0	0	0	0	0	0

Bit	Symbol	Value	Description
7	AE_D		Date Alarm Enable bit (see ALARM FUNCTION)
		0	Enabled
		1	Disabled – Default value
6	X	0	Unused
5:0	Date Alarm	01 to 31	Holds the alarm value for the date, coded in BCD format.

0Fh – Weekday Alarm

This register holds the Weekday Alarm Enable bit AE_W and the alarm value for the weekday, in two binary coded decimal (BCD) digits. Values will range from 0 to 6.

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Fh	Weekday Alarm	AE_W	X	X	X	X	4	2	1
	Reset	1	0	0	0	0	0	0	0

Bit	Symbol	Value	Description
7	AE_W		Weekday Alarm Enable bit (see ALARM FUNCTION)
		0	Enabled
		1	Disabled – Default value
6:3	X	0	Unused
2:0	Weekday Alarm	0 to 6	Holds the weekday alarm value, coded in BCD format.

3.5. TIMER REGISTERS

10h – Timer Value

This register holds the current value of the Countdown Timer. It may be loaded with the desired starting value when the Countdown Timer is stopped.

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
10h	Timer Value	128	64	32	16	8	4	2	1
	Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Value	Description
7:0	Timer Value	00h to FFh	Countdown Timer Value (see COUNTDOWN TIMER FUNCTION)

Countdown Period in seconds:

$$\text{Countdown Period} = \frac{\text{Timer Value}}{\text{Timer Clock Frequency}}$$

11h – Timer Mode

This register controls the Countdown Timer function.

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
11h	Timer Mode	X	X	X	TD		TE	TIE	TI_TP
	Reset	0	0	0	1	1	0	0	0

Bit	Symbol	Value	Description
7:5	X	0	Unused
4:3	TD		Timer Clock Frequency (see COUNTDOWN TIMER FUNCTION)[1]
		00	4.096 kHz
		01	64 Hz[2]
		10	1 Hz[2]
		11	1/60 Hz – Default value[2]
2	TE		Timer Enable
		0	Disabled – Default value
		1	Enabled
1	TIE		Timer Interrupt Enable
		0	No interrupt generated from timer. – Default value
		1	Interrupt generated from timer.
0	TI_TP		Timer Interrupt Mode. How the setting of TI_TP and the Timer Flag TF can affect the $\overline{INT}$ pulse generation is explained in sections COUNTDOWN TIMER FUNCTION and MINUTE AND HALF MINUTE INTERRUPT FUNCTION.
		0	Interval Mode. Interrupt follows Timer Flag TF. – Default value
		1	Pulse Mode. Interrupt generates a pulse.

(1) When not in use, the TD field is recommended to be set to 11 (1⁄60 Hz) for power saving.
(2) Time periods can be affected by compensation pulses (64 Hz only in MODE = 1), (see FREQUENCY OFFSET COMPENSATION).

3.6. REGISTER RESET VALUES SUMMARY

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	Control1	0	0	0	0	0	0	0	0
01h	Control2	0	0	0	0	0	0	0	0
02h	Offset	0	0	0	0	0	0	0	0
03h	RAM	0	0	0	0	0	0	0	0
04h	Seconds	1	0	0	0	0	0	0	0
05h	Minutes	0	0	0	0	0	0	0	0
06h	Hours (24h / 12h)	0	0	0	0	0	0	0	0
07h	Date	0	0	0	0	0	0	0	1
08h	Weekday	0	0	0	0	0	1	1	0
09h	Month	0	0	0	0	0	0	0	1
0Ah	Year	0	0	0	0	0	0	0	0
0Bh	Seconds Alarm	1	0	0	0	0	0	0	0
0Ch	Minutes Alarm	1	0	0	0	0	0	0	0
0Dh	Hours Alarm (24h / 12h)	1	0	0	0	0	0	0	0
0Eh	Date Alarm	1	0	0	0	0	0	0	0
0Fh	Weekday Alarm	1	0	0	0	0	0	0	0
10h	Timer Value	0	0	0	0	0	0	0	0
11h	Timer Mode	0	0	0	1	1	0	0	0

RV-8263-C8 resets to:

Time (hh:mm:ss)	=	00:00:00
Date (YY-MM-DD)	=	00-01-01
Weekday	=	Weekday 7
Mode	=	RTC clock runs, 24 h mode
Pins	=	CLKOUT Frequency = 32.768 kHz (when CLKOE is HIGH)
Offset	=	0
Alarms	=	disabled
Timer	=	disabled, Timer Clock Frequency = 1/60 Hz
Interrupts	=	disabled

4. DETAILED FUNCTIONAL DESCRIPTION

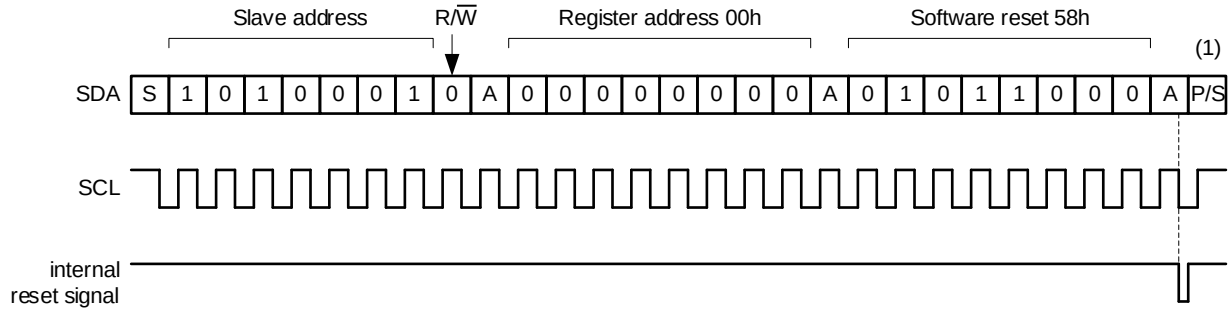
4.1. POWER ON RESET (POR)

The power on reset (POR) is generated at start-up. All registers including the Counter Registers are initialized to their reset values (see REGISTER RESET VALUES SUMMARY).
There is a small probability that the registers of the RV-8263-C8 are corrupted after an automatic power-on reset if the device is powered up with a residual V_{DD} level. For a correct POR it is required that the V_{DD} starts at zero volts at power up or upon power cycling to ensure that the registers are not corrupted.
If a valid POR cannot be performed, the reset must be initiated with the software reset command after power-up (i.e. when power is stable). See following section SOFTWARE RESET.

4.2. SOFTWARE RESET

Beside the POR, a reset can also be initiated with the software reset command. Software reset command requires a combination of the bits 6, 4, and 3 in register Control1 (00h) set to 1 and all other bits to 0 by sending the bit sequence 01011000 (58h), see following Figure.

Software reset command:



(1) After sending the software reset command, it is recommended to re-initialize the interface by an I²C STOP condition followed by an I²C START condition.

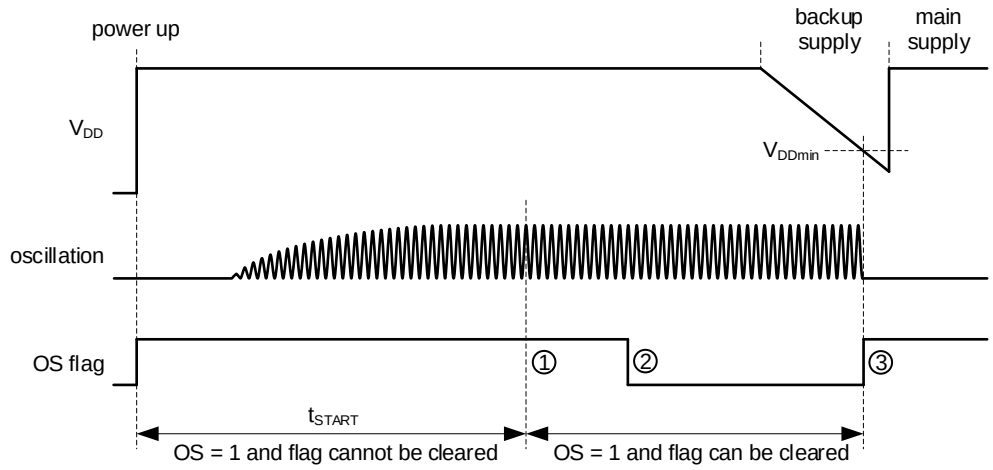
In reset state all registers are set according to the Table in section REGISTER RESET VALUES SUMMARY and the address pointer points to no address.

4.3. OSCILLATOR STOP FLAG

When the oscillator of the RV-8263-C8 is stopped, the Oscillator Stop flag OS is set. The oscillator is considered to be stopped between power up and stable crystal oscillation (start-up time t_{START}). This time can be in a range of typical 200 ms to maximal 2 s depending on temperature and supply voltage.

The flag remains set until cleared by command (see following Figure). If the flag cannot be cleared, then the oscillator is not running. This method can be used to monitor the oscillator and to determine if the supply voltage has reduced to the point where oscillation fails.

OS flag:

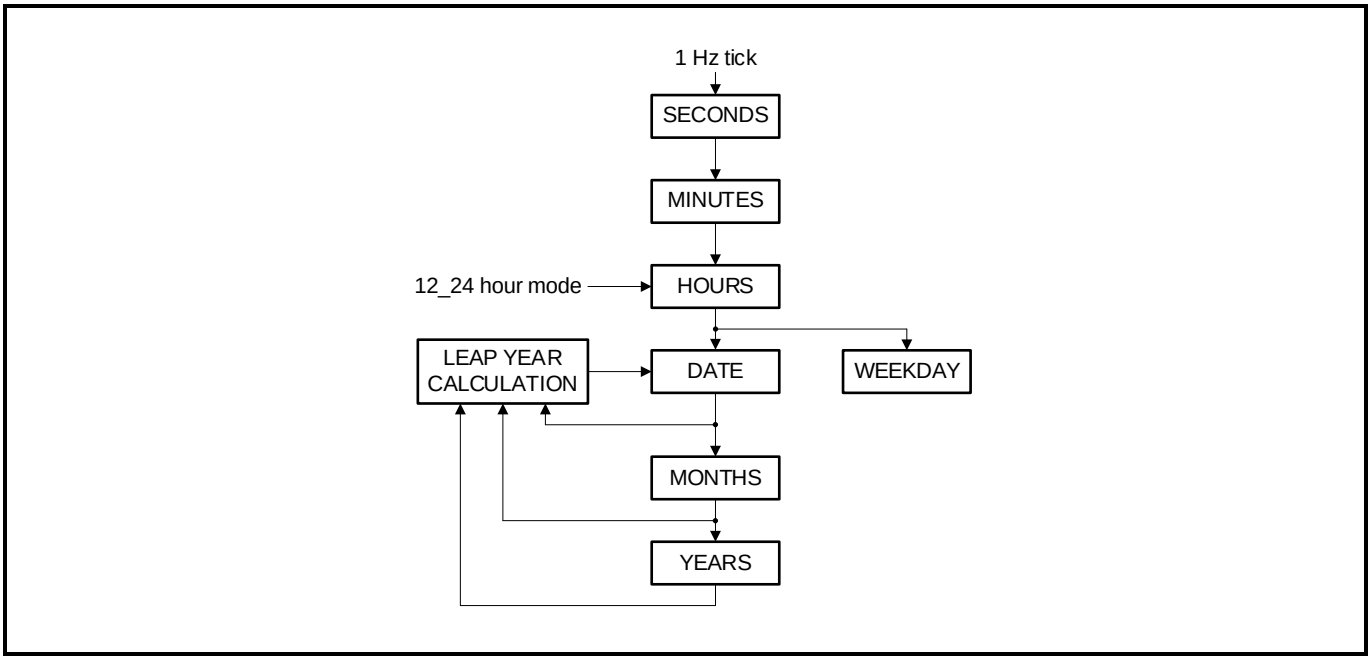


① Oscillation now stable.
② OS flag cleared by software.
③ OS flag set when oscillator stops.

4.4. SETTING AND READING THE TIME

The following Figure shows the data flow and data dependencies starting from the 1 Hz clock tick.

Data flow for the time function:



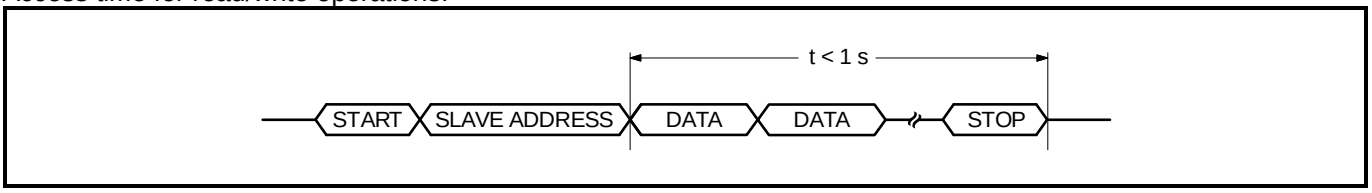
During read/write operations, the time counting registers (memory locations 04h through 0Ah) are frozen for 1 second.

The freezing prevents:

- Faulty reading of the clock and calendar during a carry condition
- Incrementing the time registers during the read cycle

When the read/write access has been terminated within 1 second (t < 1 s), the time circuit is de-frozen immediately and any pending request to increment the time counters that occurred during the read/write access is correctly applied. Maximal one 1 Hz tick can be handled.
When the read/write access last longer than 1 second, the time circuit is de-frozen automatically after 1 second in order not to miss 1 Hz ticks and the lost 1 Hz ticks cannot be handled completely. Therefore, each interface communication has to be correctly terminated within 1 second (see following Figure).

Access time for read/write operations:



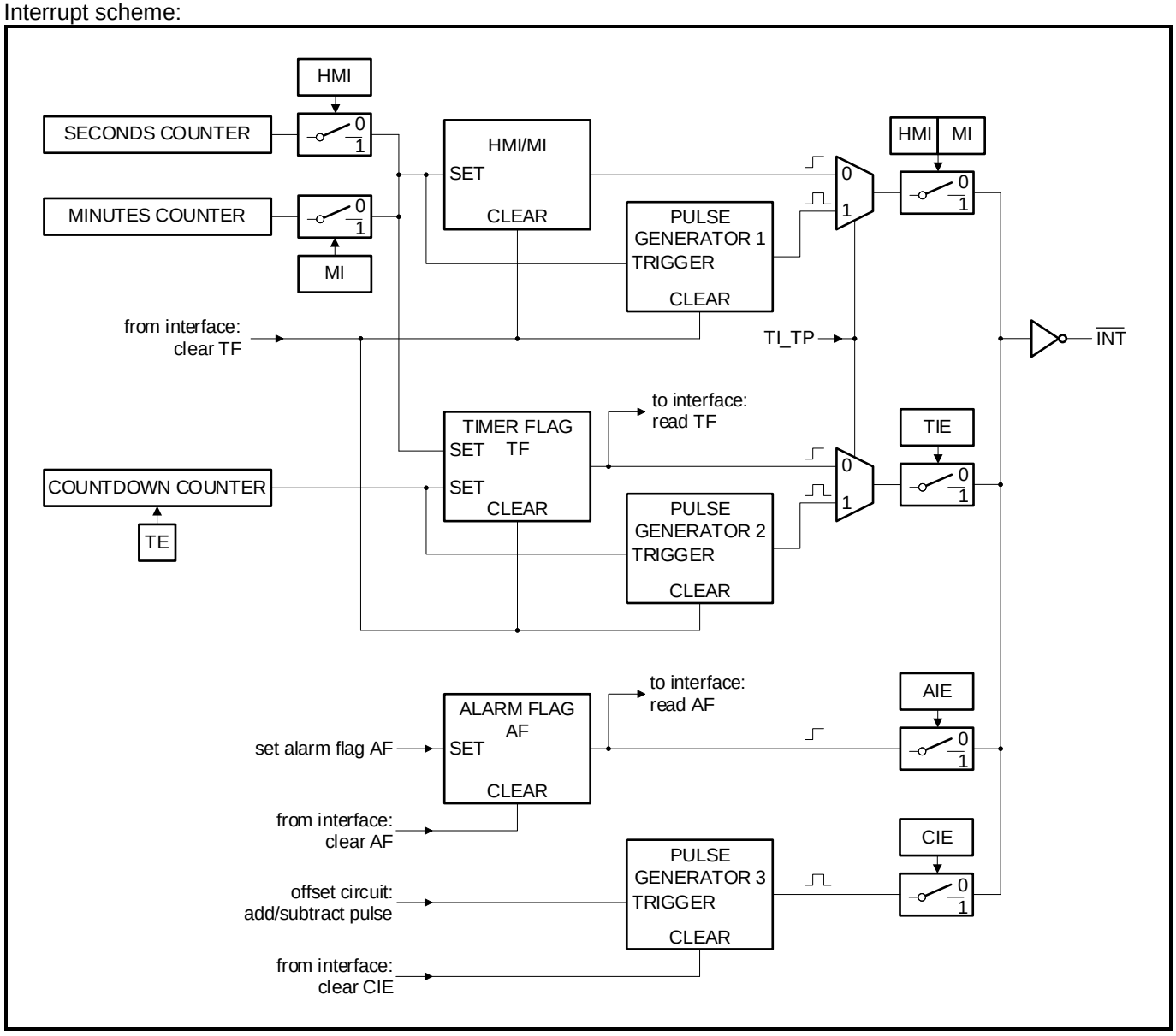
Because of this method, it is very important to make a read or write access in one go, that is, setting or reading seconds through to year should be made in one single access. Failing to comply with this method could result in the time becoming corrupted.

4.5. INTERRUPT OUTPUT

The interrupt pin $\overline{INT}$ can be triggered by four different functions:

- ALARM FUNCTION
- COUNTDOWN TIMER FUNCTION
- MINUTE AND HALF MINUTE INTERRUPT FUNCTION
- COMPENSATION INTERRUPT FUNCTION

Interrupt scheme:

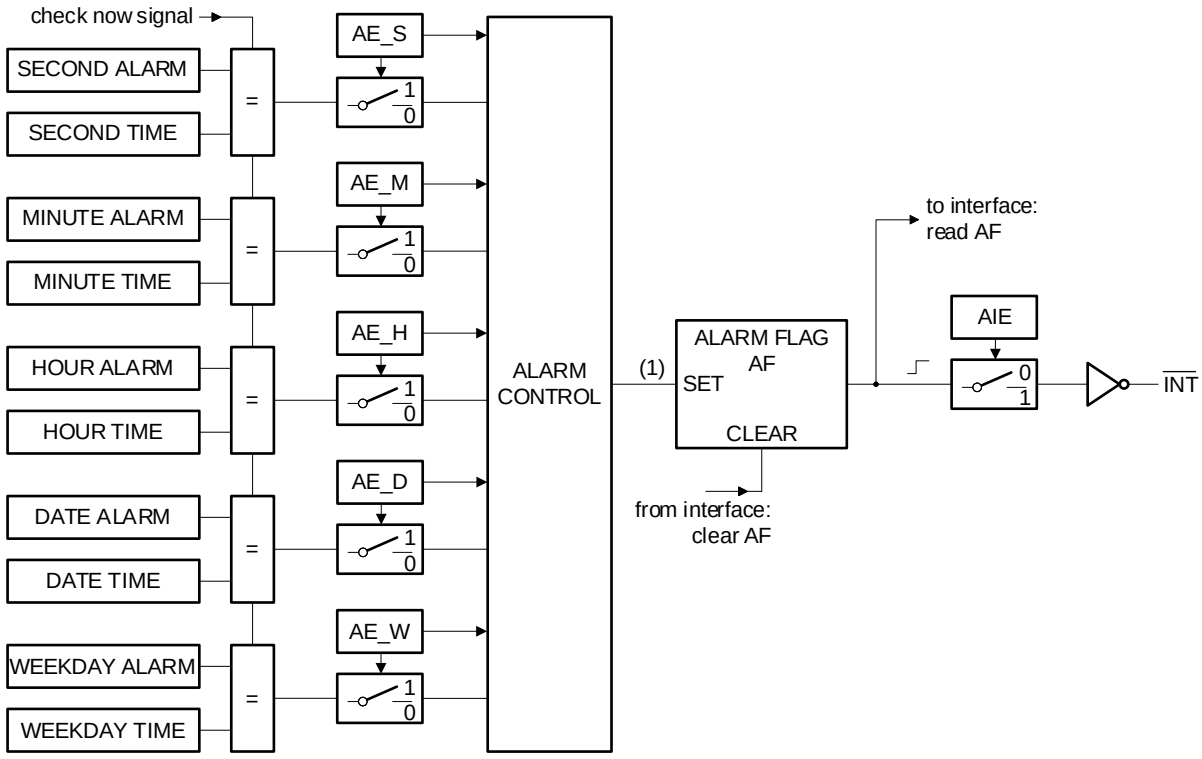


4.6. ALARM FUNCTION

By clearing the alarm enable bit (AE_x) of one or more of the alarm registers, the corresponding alarm condition(s) are active. When an alarm occurs, AF is set logic 1. The asserted AF can be used to generate an interrupt ($\overline{INT}$). The AF is cleared by command.

The registers at addresses 0Bh through 0Fh contain alarm information. When one or more of these registers is loaded with second, minute, hour, date or weekday, and its corresponding AE_x is logic 0, then that information is compared with the current second, minute, hour, date, and weekday. When all enabled comparisons first match, the Alarm Flag (AF in CONTROL REGISTERS, 01h – Control2) is set logic 1.

Alarm function block diagram:



(1) Only when all enabled alarm settings are matching.
It is only on increment to a matched case that the Alarm Flag is set.

4.6.1. ALARM INTERRUPT

The generation of interrupts from the alarm function is controlled via bit AIE. If bit AIE is enabled, the $\overline{INT}$ pin follows the condition of bit AF. AF remains set until cleared by command. Once AF has been cleared, it will only be set again when the time increments to match the alarm condition once more. Alarm registers which have their AE_x bit at logic 1 are ignored.

4.7. COUNTDOWN TIMER FUNCTION

4.7.1.TIMER FLAG TF

The Timer Flag (bit TF) is set logic 1 on the first trigger of the Countdown Timer or the MI and HMI Interrupt. The purpose of the flag is to allow the controlling system to interrogate what caused the interrupt: Timer/MI/HMI or Alarm. The flag can be read and cleared by command.

The status of the Timer Flag TF can affect the $\overline{INT}$ pulse generation depending on the setting of TI_TP (see TIMER REGISTERS, 11h – Timer Mode):

4.7.2.TIMER INTERRUPT MODE TI_TP

When Interrupt is in Interval Mode (TI_TP = 0):

- only one Interrupt after the first countdown when TF is not cleared
- the $\overline{INT}$ generation follows the TF flag
- TF stays set until it is cleared
- If TF is not cleared before the next coming interrupt, no $\overline{INT}$ is generated

When Interrupt is in Timer Pulse Mode (TI_TP = 1):

- the Countdown Timer runs in a repetitive loop and keeps generating periodic interrupts
- an $\overline{INT}$ pulse is generated independent of the status of the Timer Flag TF
- TF stays set until it is cleared.
- TF does not affect $\overline{INT}$

4.7.3.PULSE GENERATOR 2

When the Timer Pulse Mode is activated (TI_TP = 1) the Pulse Generator 2 for the Countdown Timer Interrupt uses an internal clock and is dependent on the selected Timer Clock Frequency for the countdown timer and on the Timer Value. As a consequence, the width of the interrupt pulse varies (see following Table). The pulse widths are not affected by the Offset Mode (bit MODE). TF and $\overline{INT}$ become active simultaneously.

$\overline{INT}$ pulse width when using Countdown Timer:

Timer Clock Frequency	**$\overline{INT}$ pulse width**	
	Timer Value = 1(1)	**Timer Value > 1**(1)
4.096 kHz	122 µs	244 µs
64 Hz	7.812 ms	15.625 ms
1 Hz	15.625 ms	15.625 ms
1/60 Hz	15.625 ms	15.625 ms

(1) Timer Value = loaded countdown value. Timer stops when Timer Value = 0.

4.7.4.USE OF THE COUNTDOWN TIMER

The timer has four selectable source clocks allowing for countdown periods in the range from 244 µs to 4 hours 15 min. For periods longer than 4 hours, the alarm function can be used.

Timer Clock Frequency and timer periods:

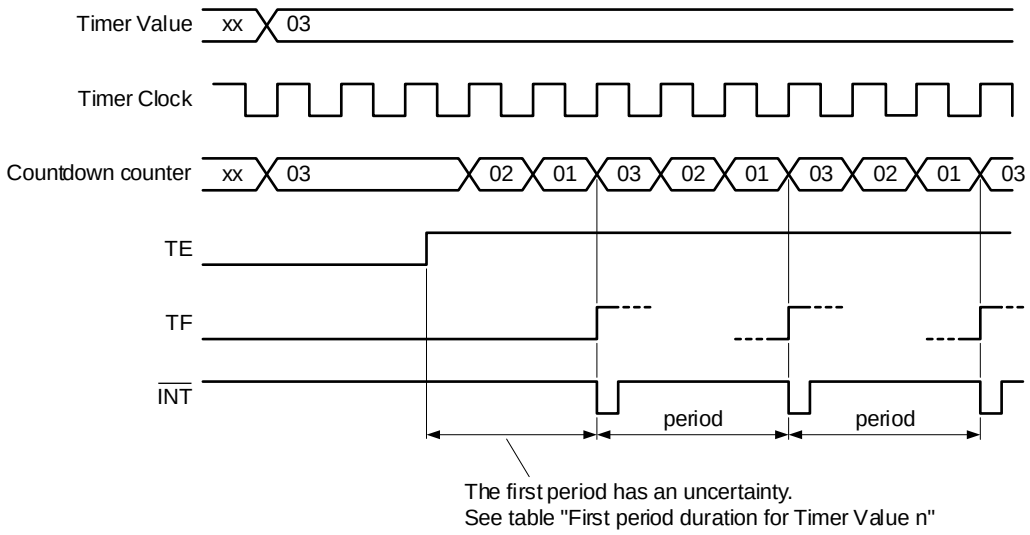
TD	Timer Clock Frequency(1)	Period	
		Minimum Period, Timer Value = 1	Maximum Period, Timer Value = 255
00	4.096 kHz	244 µs	62.256 ms
01	64 Hz(2)	15.625 ms	3.984 s
10	1 Hz(2)	1 s	255 s
11	1/60 Hz(2)	60 s	4 hours 15 min

(1) When not in use, the TD field is recommended to be set to 11 (1/60 Hz) for power saving.
(2) Time periods can be affected by compensation pulses (64 Hz only in MODE = 1), (see FREQUENCY OFFSET COMPENSATION).

Note that all timings are generated from the 32.768 kHz oscillator and therefore, based on the frequency characteristics specified for the device, have a temperature profile with a parabolic frequency deviation which can result in a change of up to 150 ppm across the entire operating temperature range of -40°C to 85°C (max. ± 20 ppm at 25°C).

The timer counts down from the software-loaded 8-bit binary Timer Value in register 10h. Timer Values from 1 to 255 are valid. Loading the counter with 0 stops the timer.
When the counter decrements from 1, the Timer Flag (bit TF in register Control2) is set and the counter automatically re-loads and starts the next timer period.

General countdown timer behavior:



In this example, it is assumed that the Timer Flag TF is cleared before the next countdown period expires and that the pin $\overline{INT}$ is set to Pulse Mode (TI_TP bit = 1).

If a new Timer Value is written before the end of the current timer period, then this value takes immediate effect. It is not recommended changing the Timer Value without first disabling the counter by setting bit TE logic 0. The update of the Timer Value is asynchronous to the Timer Clock.
Therefore changing it without setting bit TE logic 0 may result in a corrupted value loaded into the countdown counter. This results in an undetermined countdown period for the first period. The Timer Value will, however, be correctly stored and correctly loaded on subsequent timer periods.

When the TF flag is set, an interrupt signal on $\overline{INT}$ is generated if this mode is enabled. See Section INTERRUPT OUTPUT for details on how the interrupt can be controlled.

When starting the timer for the first time, the first period has an uncertainty. The uncertainty is a result of the enable instruction being generated from the interface clock which is asynchronous from the Timer Clock Frequency. Subsequent timer periods do not have such deviation. The amount of deviation for the first timer period depends on the chosen source clock, see following Table.

First period duration for Timer Value n[(1)]:

TD	Timer Clock Frequency	First period duration		Subsequent periods duration
		Minimum Period	Maximum Period	
00	4.096 kHz	(n – 1) * 244 µs	n * 244 µs	n * 244 µs
01	64 Hz	(n – 1) * 15.625 ms	n * 15.625 ms	n * 15.625 ms
10	1 Hz	(n – 1) * 1 s + 265 ms	(n – 1) * 1 s + 280 ms	n * 1 s
11	1/60 Hz	(n – 1) * 60 s + 59.212 s	(n – 1) * 60 s + 59.216 s	n * 60 s

(1) Timer Values n from 1 to 255 are valid. Loading the counter with 0 stops the timer.

At the end of every countdown, the timer sets the countdown Timer Flag (bit TF in register Control2). Bit TF can only be cleared by command. The asserted bit TF can be used to generate an interrupt at pin $\overline{INT}$. The interrupt may be generated as a pulsed signal every countdown period or as a permanently active signal which follows the condition of bit TF. Bit TI_TP is used to control this mode selection and the interrupt output may be disabled with bit TIE (see TIMER REGISTERS, 11h – Timer Mode; and Figure “General countdown timer behavior” above).

When reading the Timer Value, the current countdown value is returned and **not** the initial Timer Value. Since it is not possible to freeze the countdown timer counter during read back, it is recommended to read the register twice and check for consistent results.

The Timer Clock Frequencies 64 Hz (only in MODE = 1), 1 Hz and 1⁄60 Hz can be affected by the Offset register. The duration of a programmed period varies according to when the offset is initiated (OFFSET not 00h). For example, if a 100 s timer is set using the 1 Hz clock as source, then some 100 s periods will contain compensation pulses and therefore be longer or shorter depending on the setting of the Offset register (see FREQUENCY OFFSET COMPENSATION).

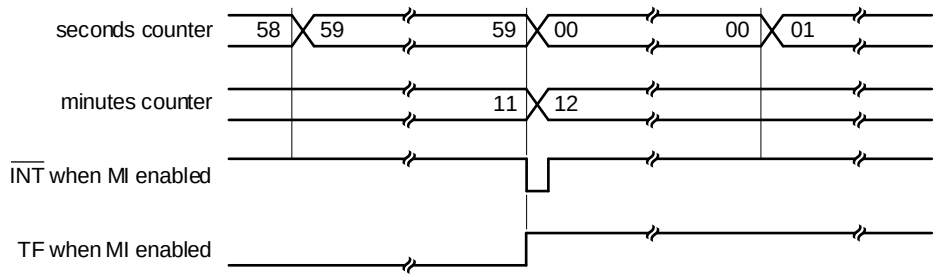
4.8. MINUTE AND HALF MINUTE INTERRUPT FUNCTION

The Minute Interrupt (bit MI) and Half Minute Interrupt (bit HMI) are pre-defined timers for generating interrupt pulses on pin $\overline{INT}$ (see following Figure). The timers are running in sync with the seconds counter (see TIME AND DATE REGISTERS, 04h - Seconds).

The minute and half minute interrupts must only be used when the frequency offset is set to normal mode (MODE = 0), see FREQUENCY OFFSET COMPENSATION. In normal mode, the interrupt pulses on pin $\overline{INT}$ are 15.625 ms wide.

When starting MI, the first interrupt will be generated after 1 second to 59 seconds. When starting HMI, the first interrupt will be generated after 1 second to 29 seconds.
Subsequent periods do not have such a delay. The timers can be enabled independently from one another. However, a Minute Interrupt enabled on top of a Half Minute Interrupt is not distinguishable.

$\overline{INT}$ example for MI:



In this example, the TF flag is not cleared after an interrupt and the pin $\overline{INT}$ is set to Pulse Mode (TI_TP bit = 1).

Effect of bits MI and HMI on $\overline{INT}$ generation:

Minute Interrupt (bit MI)	Half Minute Interrupt (bit HMI)	Result
0	0	No interrupt generated
1	0	Interrupt every minute
0	1	Interrupt every 30 seconds
1	1	

The duration of the timer is affected by the register Offset (see CONTROL REGISTERS, 02h – Offset Register). Only when OFFSET has the value 00h the periods are consistent.

4.8.1.PULSE GENERATOR 1

When the Timer Pulse Mode is activated (TI_TP = 1) the Pulse Generator 1 for the HMI and MI Interrupt Function uses an internal clock.
The minute and half minute interrupts must only be used when the frequency offset is set to normal mode (MODE = 0). In normal mode, the interrupt pulses on pin $\overline{INT}$ are 15.625 ms wide. TF and $\overline{INT}$ become active simultaneously.

4.9. FREQUENCY OFFSET COMPENSATION

The RV-8263-C8 incorporates an Offset register (see CONTROL REGISTERS, 02h – Offset Register) which can be used by customer to compensate the frequency offset of the 32.768 kHz oscillator which allows implementing functions, such as:

- Improve time accuracy
- Aging compensation

02h – Offset Register:

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
02h	Offset	MODE	OFFSET						
	Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Value	Description
7	MODE		Offset Mode
		0	Normal Mode: Offset is made once every two hours.
		1	Fast Mode: Offset is made every 4 minutes.
6:0	OFFSET	-64 to +63	Offset value. For MODE = 0, each LSB introduces an offset of 4.34 ppm. For MODE = 1, each LSB introduces an offset of 4.069 ppm. The values of 4.34 ppm and 4.069 ppm are based on a nominal 32.768 kHz clock. The offset value is coded in two's complement giving a range of +63 LSB to -64 LSB.

OFFSET	OFFSET compensation value in decimal	Compensation pulses in steps	CLKOUT offset value in ppm(1)	
			Normal Mode MODE = 0	Fast Mode MODE = 1
0111111	63	+63	+273.420	+256.347
0111110	62	+62	+269.080	+252.278
:	:	:	:	:
0000001	1	+1	+4.340	+4.069
0000000	0	0	0	0
1111111	127	-1	-4.340	-4.069
1111110	126	-2	-8.680	-8.138
:	:	:	:	:
1000001	65	-63	-273.420	-256.347
1000000	64	-64	-277.760	-260.416

(1) The frequency offset measured at CLKOUT pin can be compensated by computing the compensation value OFFSET and writing it into the Offset register (see OFFSET COMPENSATION CALCULATION WORKFLOW).

The compensation is made by adding or subtracting clock compensation pulses. The affects to the different frequencies are listed below.

CLKOUT frequencies:

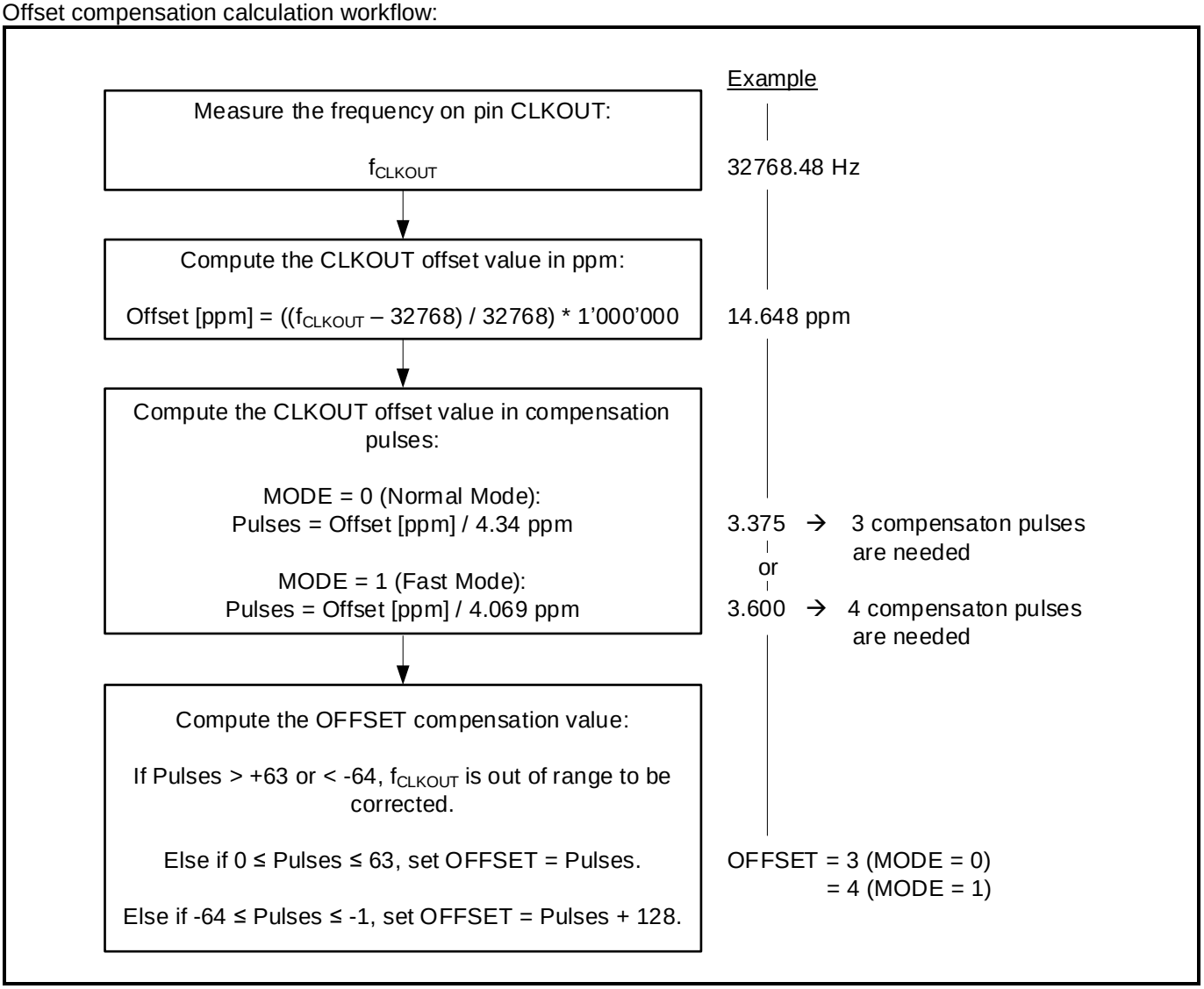
- 1 Hz can be affected
- 1.024 kHz to 32.768 kHz are not affected

Timer Clock frequencies:

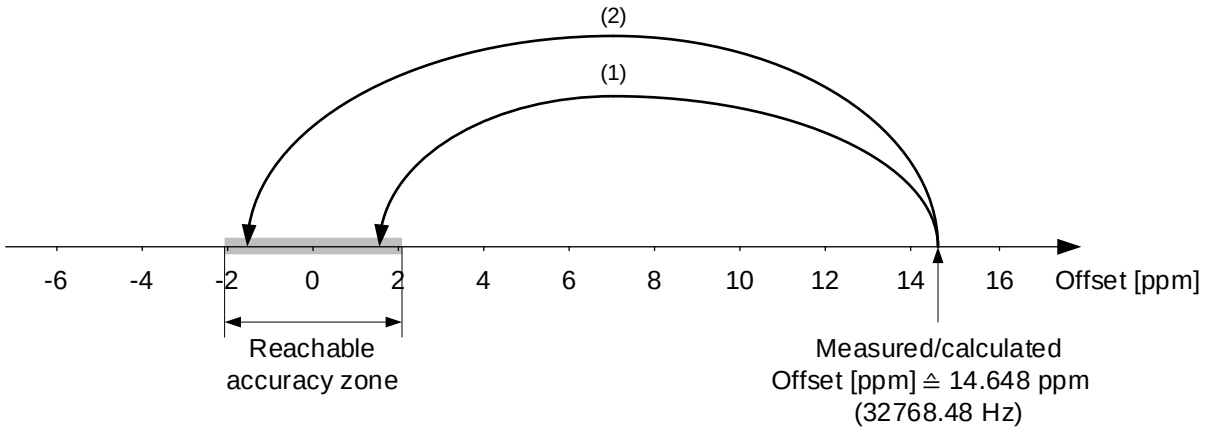
- MODE = 0 (Normal Mode):
  - 1/60 Hz and 1 Hz can be affected
  - 64 Hz and 4.096 kHz are not affected
- MODE = 1 (Fast Mode):
  - 1/60 Hz, 1 Hz and 64 Hz can be affected
  - 4.096 kHz is not affected

4.9.1.OFFSET COMPENSATION CALCULATION WORKFLOW

Offset compensation calculation workflow:



Result of the offset compensation (Example):



With the offset compensation the accuracy of ±2.17 ppm (0.5 * offset per LSB) can be reached (see CONTROL REGISTERS, 02h – Offset Register).
±1 ppm corresponds to a time deviation of 0.0864 seconds per day.

(1) MODE = 0: Deviation after compensation = Offset [ppm] – compensation pulses * 4.34 ppm
= 14.648 ppm – 3 * 4.34 ppm = +1.628 ppm
(2) MODE = 1: Deviation after compensation = Offset [ppm] – compensation pulses * 4.069 ppm
= 14.648 ppm – 4 * 4.069 ppm = -1.628 ppm

4.10. COMPENSATION INTERRUPT FUNCTION

It is possible to monitor when compensation pulses are applied. To enable Compensation Interrupt generation, bit CIE (register Control1) has to be set logic 1. At every compensation cycle a pulse is generated on pin $\overline{INT}$ by the Pulse Generator 3. The pulse width depends on the Offset Mode (MODE bit). If multiple compensation pulses are applied, an interrupt pulse is generated for each compensation pulse applied.

4.10.1. COMPENSATION PULSES WHEN MODE = 0 (NORMAL MODE)

The compensation is triggered once every two hours and then compensation pulses are applied once per minute until the programmed offset value has been compensated.

Compensation pulses when MODE = 0:

Compensation pulses in steps	Update every n^{th} hour	Minute	Compensation pulses on $\overline{INT}$ per minute(1)
+1 or -1	2	00	1
+2 or -2	2	00 and 01	1
+3 or -3	2	00, 01, and 02	1
:	:	:	:
+59 or -59	2	00 to 58	1
+60 or -60	2	00 to 59	1
+61 or -61	2	00 to 59	1
	2nd and next hour	00	1
+62 or -62	2	00 to 59	1
	2nd and next hour	00 and 01	1
+63 or -63	2	00 to 59	1
	2nd and next hour	00, 01, and 02	1
-64	2	00 to 59	1
	2nd and next hour	00, 01, 02, and 03	1

(1) When MODE = 0, the compensation pulses on pin $\overline{INT}$ are 15.625 ms wide.

In MODE = 0, CLKOUT and Timer Clock frequencies < 64 Hz are affected by the compensation pulses.

Effect of compensation pulses on frequencies when MODE = 0:

Frequency	Effect of compensation
CLKOUT	
32.768 kHz	no effect
16.384 kHz	no effect
8.192 kHz	no effect
4.096 kHz	no effect
2.048 kHz	no effect
1.024 kHz	no effect
1 Hz	Frequency affected
Timer Clock	
4.096 kHz	no effect
64 Hz	no effect
1 Hz	Periods affected
1/60 Hz	Periods affected

4.10.2. COMPENSATION PULSES WHEN MODE = 1 (FAST MODE)

The compensation is triggered once every four minutes and then compensation pulses are applied once per second up to a maximum of 60 pulses. When compensation values greater than 60 pulses are used, additional compensation pulses are made in the 59th second.

Clock compensation is made more frequently in MODE = 1; resulting in slightly higher power consumption.

Compensation pulses when MODE = 1:

Compensation pulses in steps	Update every nth minute	Second	Compensation pulses on $\overline{INT}$ per second(1)
+1 or -1	4	00	1
+2 or -2	4	00 and 01	1
+3 or -3	4	00, 01, and 02	1
:	:	:	:
+59 or -59	4	00 to 58	1
+60 or -60	4	00 to 59	1
+61 or -61	4	00 to 58	1
	4	59	2
+62 or -62	4	00 to 58	1
	4	59	3
+63 or -63	4	00 to 58	1
	4	59	4
-64	4	00 to 58	1
	4	59	5

(1) When MODE = 1, the compensation pulses on pin $\overline{INT}$ are 977 µs wide. For multiple pulses, they are repeated at an interval of 1.953 ms.

In MODE = 1, CLKOUT or Timer Clock frequencies < 1.024 kHz are affected by the compensation pulses.

Effect of compensation pulses on frequencies when MODE = 1:

Frequency	Effect of compensation
CLKOUT	
32.768 kHz	no effect
16.384 kHz	no effect
8.192 kHz	no effect
4.096 kHz	no effect
2.048 kHz	no effect
1.024 kHz	no effect
1 Hz	Frequency affected
Timer Clock	
4.096 kHz	no effect
64 Hz	Periods affected
1 Hz	Periods affected
1/60 Hz	Periods affected

4.11. CLKOUT FREQUENCY SELECTION

A programmable square wave is available at pin CLKOUT. Operation is controlled by the FD field in the register Control2. Frequencies of 32.768 kHz (default) down to 1 Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the crystal oscillator.

Pin CLKOUT is a push-pull output and enabled at power-on. CLKOUT can be disabled by setting the FD field to 111 or by setting CLKOE LOW. When disabled, the CLKOUT is LOW.

The duty cycle of the selected clock is not controlled. However, due to the nature of the clock generation, all are 50 : 50 except the 32.768 kHz frequency.

The STOP bit function can also affect the CLKOUT signal, depending on the selected frequency. When the STOP bit is set logic 1, the CLKOUT pin generates a continuous LOW for those frequencies that can be stopped (for more details, see STOP BIT FUNCTION).

FD	CLKOUT Frequency	Typical duty cycle	Effect of STOP bit
000	32.768 kHz – Default value	50 ±10 %	no effect
001	16.384 kHz	50 %	no effect
010	8.192 kHz	50 %	no effect
011	4.096 kHz	50 %	CLKOUT = LOW
100	2.048 kHz	50 %	CLKOUT = LOW
101	1.024 kHz	50 %	CLKOUT = LOW
110	1 Hz (1)	50 %	CLKOUT = LOW
111	CLKOUT = LOW	-	-

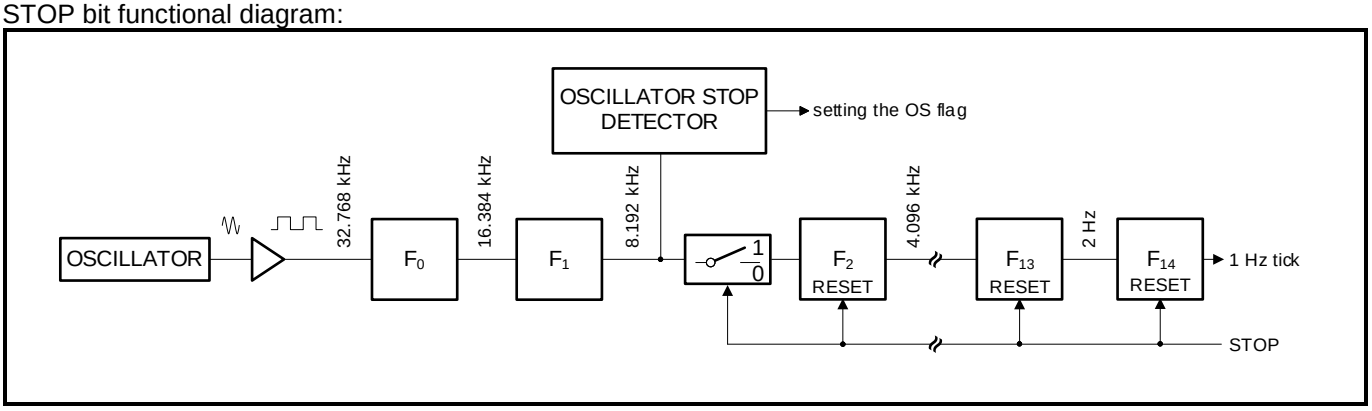
(1) 1 Hz clock pulses are affected by compensation pulses (see FREQUENCY OFFSET COMPENSATION).

4.12. STOP BIT FUNCTION

The function of the STOP bit is to allow for accurate starting of the time circuits.

The STOP bit function causes the upper part of the prescaler (F_2 to F_{14}) to be held in reset and thus no 1 Hz ticks are generated. The STOP bit function will not affect the CLKOUT of 32.768 kHz, 16.384 kHz and 8.192 kHz (see also CLKOUT FREQUENCY SELECTION).

STOP bit functional diagram:



The time circuits can then be set and do not increment until the STOP bit is released (see following Table and Figure).

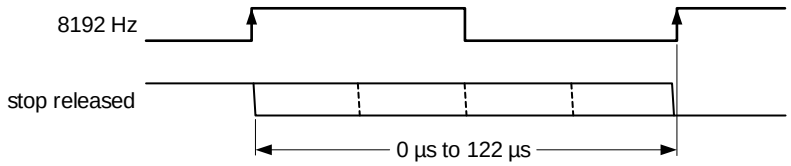
First increment of time circuits after STOP bit release:

STOP bit	Prescaler bits [1] F_0F_1-F_2 to F_{14}	1 Hz tick	Time hh:mm:ss	Comment
Clock is running normally				
0	01-0 0001 1101 0100		12:45:12	Prescaler counting normally
STOP bit is activated by user. F_0F_1 are not reset and values cannot be predicted externally				
1	XX-0 0000 0000 0000		12:45:12	Prescaler is reset; time circuits are frozen
New time is set by user				
1	XX-0 0000 0000 0000		08:00:00	Prescaler is reset; time circuits are frozen
STOP bit is released by user				
0	XX-0 0000 0000 0000	0.507 813 to 0.507 935 s	08:00:00	Prescaler is now running
	XX-1 0000 0000 0000		08:00:00	-
	XX-0 1000 0000 0000		08:00:00	-
	XX-1 1000 0000 0000		08:00:00	-
	:		:	:
	11-1 1111 1111 1110		08:00:00	-
	00-0 0000 0000 0001		08:00:01	0 to 1 transition of F_{14} increments the time circuits
	10-0 0000 0000 0001		08:00:01	-
	:		:	:
	11-1 1111 1111 1111		08:00:01	-
	00-0 0000 0000 0000	1.000 000 s	08:00:01	-
	10-0 0000 0000 0000		08:00:01	-
	:		:	:
	11-1 1111 1111 1110		08:00:01	-
	00-0 0000 0000 0001		08:00:02	0 to 1 transition of F_{14} increments the time circuits
	10-0 0000 0000 0001		08:00:02	-

1) F_0 is clocked at 32.768 kHz.

The lower two stages of the prescaler (F_0 and F_1) are not reset. And because the I²C-Bus is asynchronous to the crystal oscillator, the accuracy of restarting the time circuits is between zero and one 8.192 kHz cycle (see following Figure).

STOP bit release timing:



The first increment of the time circuits is between 0.507813 s and 0.507935 s after STOP bit is released. The uncertainty is caused by the prescaler bits F_0 and F_1 not being reset (see Table above) and the unknown state of the 32 kHz clock.

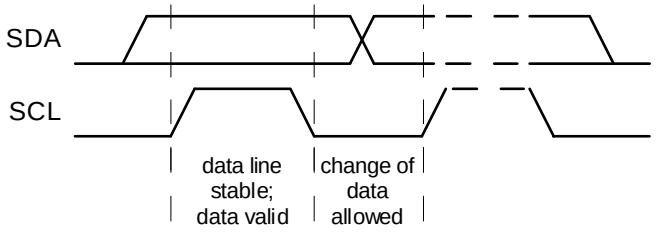
5. I²C INTERFACE

The I²C interface is for bidirectional, two-line communication between different ICs or modules. The RV-8263-C8 is accessed at addresses A2h/A3h, and supports Fast Mode (up to 400 kHz). The I²C interface consists of two lines: one bi-directional data line (SDA) and one clock line (SCL). Both lines are connected to a positive supply via pull-up resistors. Data transfer is initiated only when the interface is not busy.

5.1. BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line remains stable during the HIGH period of the clock pulse, as changes in the data line at this time are interpreted as a control signals. Data changes should be executed during the LOW period of the clock pulse (see Figure below).

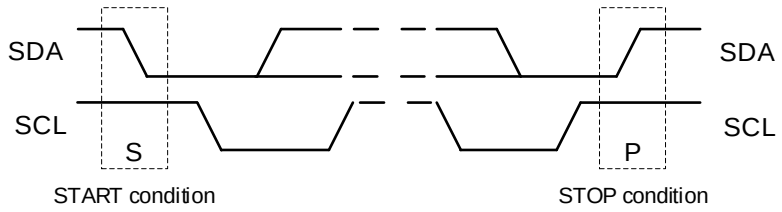
Bit transfer:



5.2. START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the START condition (S). A LOW-to-HIGH transition of the data line, while the clock is HIGH, is defined as the STOP condition (P) (see Figure below).

Definition of START and STOP conditions:



A START condition which occurs after a previous START but before a STOP is called a Repeated START condition, and functions exactly like a normal STOP followed by a normal START.

Caution:
When communicating with the RV-8263-C8 module, the series of operations from transmitting the START condition to transmitting the STOP condition should occur within **1 second**.

If this series of operations requires **1 second or longer**, the I²C bus interface will be automatically cleared and set to standby mode by the bus timeout function of the RV-8263-C8 module. Note with caution that both write and read operations are invalid for communications that occur during or after this auto clearing operation (when the read operation is invalid, all data that is read has a value of FFh).
Restarting of communications begins with transfer of the START condition again.

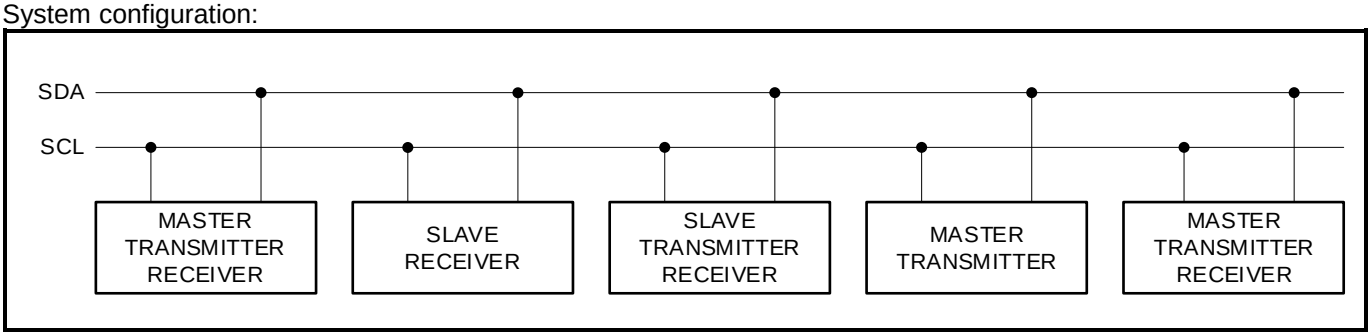
5.3. DATA VALID

After a START condition, SDA is stable for the duration of the high period of SCL. The data on SDA may be changed during the low period of SCL. There is one clock pulse per bit of data. Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between the START and STOP conditions is not limited (however, the transfer time must be no longer than 1 second). The information is transmitted byte-wise and each receiver acknowledges with a ninth bit.

5.4. SYSTEM CONFIGURATION

Since multiple devices can be connected with the I²C-bus, all I²C-bus devices have a fixed and unique device number built-in to allow individual addressing of each device.
The device that controls the I²C-bus is the Master; the devices which are controlled by the Master are the Slaves. A device generating a message is a Transmitter; a device receiving a message is the Receiver. The RV-8263-C8 acts as a Slave-Receiver or Slave-Transmitter.
Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the START procedure. The clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line.

System configuration:

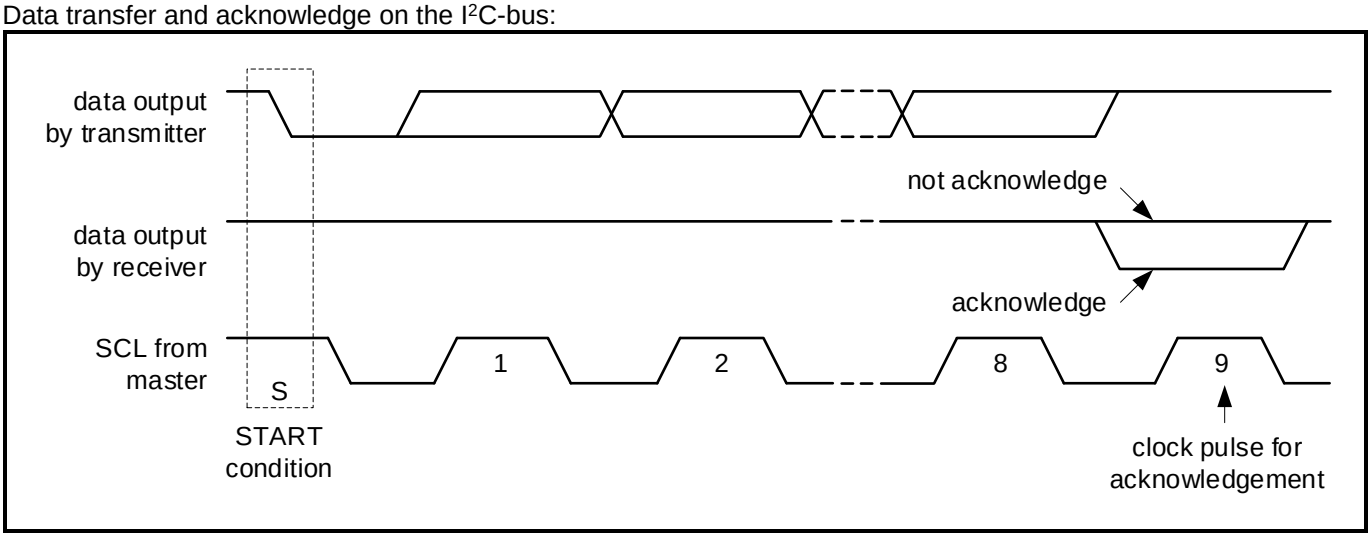


5.5. ACKNOWLEDGE

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited (however, the transfer time must be no longer than 1 second). Each byte of eight bits is followed by an acknowledge cycle.

- A slave receiver, which is addressed, must generate an acknowledge cycle after the reception of each byte.
- Also a master receiver must generate an acknowledge cycle after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse (set-up and hold times must be taken into consideration).
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge cycle on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Data transfer and acknowledge on the I²C-bus:



5.6. SLAVE ADDRESS

On the I²C-bus the 7-bit slave address 1010001b is reserved for the RV-8263-C8. The entire I²C-bus slave address byte is shown in the following table.

Slave address							R/$\overline{W}$	Transfer data
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
1	0	1	0	0	0	1	1 (R)	A3h (read)
							0 ($\overline{W}$)	A2h (write)

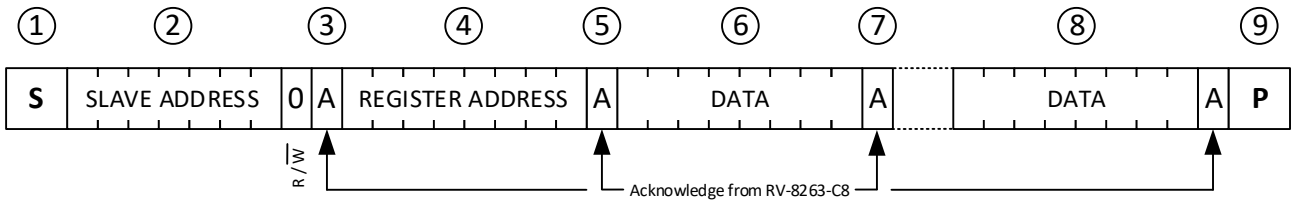
After a START condition, the I²C slave address has to be sent to the RV-8263-C8 device. The R/$\overline{W}$ bit defines the direction of the following single or multiple byte data transfer. The 7-bit address is transmitted MSB first. If this address is 1010001b, the RV-8263-C8 is selected, the eighth bit indicates a read (R/$\overline{W}$ = 1) or a write (R/$\overline{W}$ = 0) operation (results in A3h or A2h) and the RV-8263-C8 supplies the ACK. The RV-8263-C8 ignores all other address values and does not respond with an ACK.
In the write operation, a data transfer is terminated by sending either the STOP condition or the START condition of the next data transfer.

5.7. WRITE OPERATION

Master transmits to Slave-Receiver at specified address. The Register Address is an 8-bit value that defines which register is to be accessed next. After writing one byte, the Register Address is automatically incremented by 1.

Master writes to slave RV-8263-C8 at specific address:

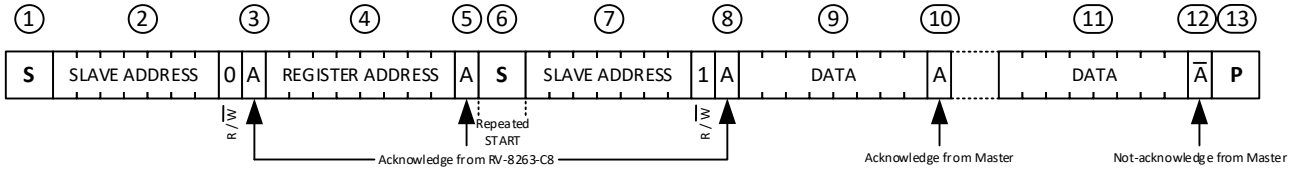
1) Master sends out the START condition.
2) Master sends out Slave Address, A2h for the RV-8263-C8; the R/$\overline{W}$ bit is a 0 indicating a write operation.
3) Acknowledgement from RV-8263-C8.
4) Master sends out the Register Address to RV-8263-C8.
5) Acknowledgement from RV-8263-C8.
6) Master sends out the Data to write to the specified address in step 4).
7) Acknowledgement from RV-8263-C8.
8) Steps 6) and 7) can be repeated if necessary.
   The address is automatically incremented in the RV-8263-C8.
9) Master sends out the STOP Condition.



5.8. READ OPERATION AT SPECIFIC ADDRESS

Master reads data from slave RV-8263-C8 at specific address:

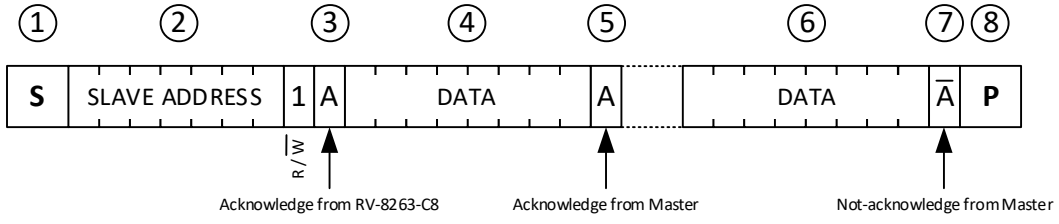
1) Master sends out the START condition.
2) Master sends out Slave Address, A2h for the RV-8263-C8; the R/$\overline{W}$ bit is a 0 indicating a write operation.
3) Acknowledgement from RV-8263-C8.
4) Master sends out the Register Address to RV-8263-C8.
5) Acknowledgement from RV-8263-C8.
6) Master sends out the Repeated START condition (or STOP condition followed by START condition).
7) Master sends out Slave Address, A3h for the RV-8263-C8; the R/$\overline{W}$ bit is a 1 indicating a read operation.
8) Acknowledgement from RV-8263-C8.
   At this point, the Master becomes a Receiver and the Slave becomes the Transmitter.
9) The Slave sends out the Data from the Register Address specified in step 4).
10) Acknowledgement from Master.
11) Steps 9) and 10) can be repeated if necessary.
    The address is automatically incremented in the RV-8263-C8.
12) The Master, addressed as Receiver, can stop data transmission by not generating an acknowledge on the last byte that has been sent from the Slave-Transmitter. In this event, the Slave-Transmitter must leave the data line HIGH to enable the Master to generate a STOP condition.
13) Master sends out the STOP condition.



5.9. READ OPERATION

Master reads data from slave RV-8263-C8 immediately after first byte:

1) Master sends out the START condition.
2) Master sends out Slave Address, A3h for the RV-8263-C8; the R/$\overline{W}$ bit is a 1 indicating a read operation.
3) Acknowledgement from RV-8263-C8.
   At this point, the Master becomes a Receiver and the Slave becomes the Transmitter.
4) The RV-8263-C8 sends out the Data from the last accessed Register Address incremented by 1.
5) Acknowledgement from Master.
6) Steps 4) and 5) can be repeated if necessary.
   The address is automatically incremented in the RV-8263-C8.
7) The Master, addressed as Receiver, can stop data transmission by not generating an acknowledge on the last byte that has been sent from the Slave-Transmitter. In this event, the Slave-Transmitter must leave the data line HIGH to enable the Master to generate a STOP condition.
8) Master sends out the STOP condition.



6. ELECTRICAL SPECIFICATIONS

6.1. ABSOLUTE MAXIMUM RATINGS

The following Table lists the absolute maximum ratings.

Absolute Maximum Ratings according to IEC 60134:

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{DD}	Power supply voltage		-0.5	6.5	V
I_{DD}	Power supply current		-50	50	mA
V_I	Input voltage		-0.5	6.5	V
V_O	Output voltage		-0.5	6.5	V
I_I	Input current	At any input	-10	10	mA
I_O	Output current	At any output	-10	10	mA
P_{TOT}	Total power dissipation			300	mW
V_{ESD}	Electrostatic discharge Voltage	HBM (1)		±5000	V
		CDM (2)		±2000	V
I_{LU}	Latch-up current	(3)		200	mA
T_{OPR}	Operating temperature		-40	85	°C
T_{STO}	Storage temperature	Stored as bare product	-55	125	°C
T_{PEAK}	Maximum reflow condition	JEDEC J-STD-020C		265	°C

(1) HBM: Human Body Model, according to JESD22-A114.
(2) CDM: Charged-Device Model, according to JESD22-C101.
(3) Latch-up testing, according to JESD78, at maximum ambient temperature ($T_{A(max)}$)

6.2. OPERATING PARAMETERS

For this Table, T_A = -40 to +85°C unless otherwise indicated. V_{DD} = 0.9 to 5.5 V, TYP values at 25°C and 3.0 V.

Operating Parameters:

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supplies						
V_{DD}	Power supply voltage	Time-keeping mode; interface inactive; f_{SCL} = 0 Hz (1)	0.9		5.5	V
		Interface active; f_{SCL} = 400 kHz (2)	1.8		5.5	
I_{DD}	V_{DD} supply current timekeeping. CLKOUT disabled; Interface inactive, f_{SCL} = 0 Hz (3)	V_{DD} = 3.0 V, T_A = 25°C		190	450	nA
		V_{DD} = 3.0 V, T_A = 50°C (4)		230	500	
		V_{DD} = 3.0 V, T_A = 85°C		450	600	
I_{DD}	V_{DD} supply current timekeeping. CLKOUT disabled; Interface active, f_{SCL} = 400 kHz	V_{DD} = 3.0 V		18	50	µA
Inputs						
V_I	Input voltage		V_{SS} -0.5		V_{DD} +0.5	V
V_{IL}	LOW level input voltage		V_{SS}		0.3 V_{DD}	V
V_{IH}	HIGH level input voltage		0.7 V_{DD}		V_{DD}	V
I_{LEAK}	Input leakage current	V_I = V_{SS} or V_{DD}		0		µA
		V_I = V_{SS} or V_{DD}, post ESD event			±0.5	µA
C_I	Input capacitance	On pins SDA, SCL and CLKOE (5)			7	pF
Outputs						
V_{OH}	HIGH level output voltage	On pin CLKOUT	0.8 V_{DD}		V_{DD}	V
V_{OL}	LOW level output voltage	On pins SDA, $\overline{INT}$, CLKOUT	V_{SS}		0.2 V_{DD}	V
I_{OH}	HIGH level output current	Output source current				
		On pin CLKOUT V_{OH} = 2.6 V, V_{DD} = 3.0 V	1	3		mA
I_{OL}	LOW level output current	Output sink current				
		On pin SDA V_{OL} = 0.4 V, V_{DD} = 3.0 V	3	8.5		mA
		On pin $\overline{INT}$ V_{OL} = 0.4 V, V_{DD} = 3.0 V	2	6		mA
		On pin CLKOUT V_{OL} = 0.4 V, V_{DD} = 3.0 V	1	3		mA

(1) For reliable oscillator start-up at power-on, V_{DD} greater than 1.2 V has to be applied. If powered up at 0.9 V, t_{START} might be a little higher, especially at high temperature. Normally the power supply is not 0.9 V at start-up and only occurs at the end of a battery discharge. V_{DD} min of 0.9 V is specified so that the customer can calculate the dimension of a battery or capacitor for a specific application. V_{DD} min of 1.2 V or greater is needed to ensure speedy oscillator start-up time.

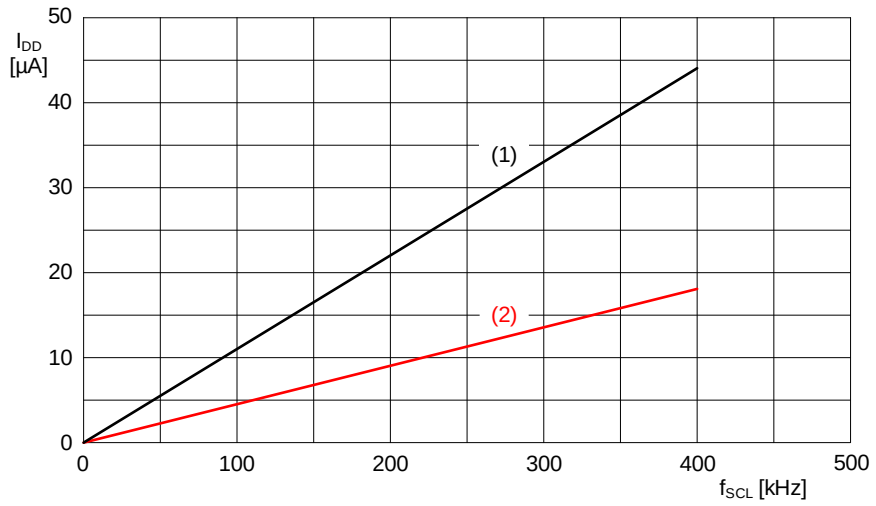
(2) 400 kHz I²C operation is production tested at 1.8 V. Design methodology allows I²C operation at 1.8 V - 5 % (1.71 V) which has been verified during product characterization on a limited number of devices.

(3) Timer source clock = 1⁄60 Hz; level of pins SCL and SDA is V_{DD} or V_{SS}.

(4) Tested on sample basis.

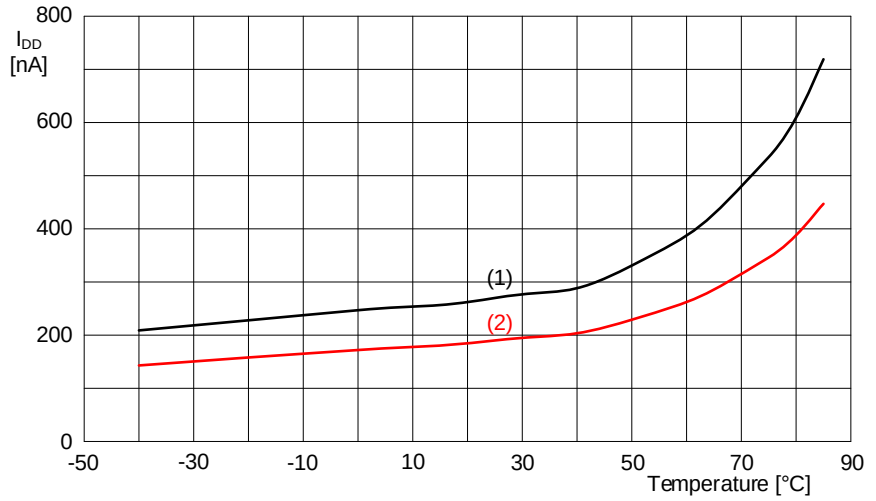
(5) Implicit by design.

I^2C active. Typical I_{DD} with respect to f_{SCL}:



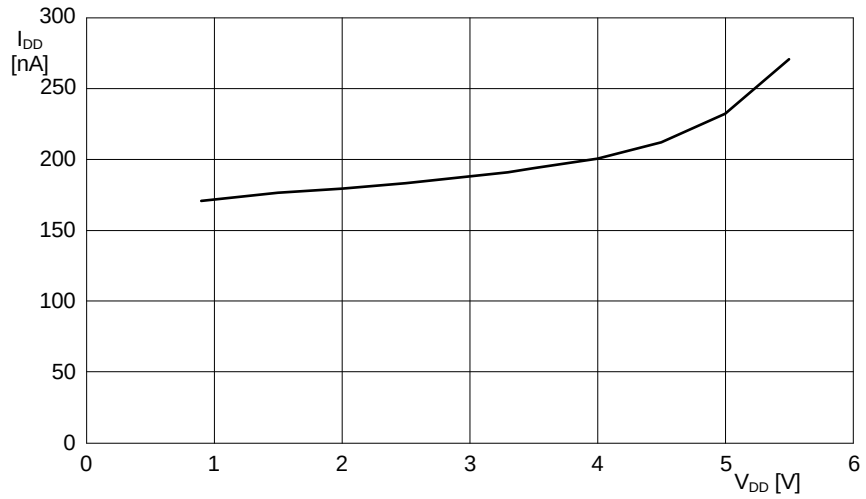
T_A = 25°C; CLKOUT disabled.
(1) V_{DD} = 5.5 V.
(2) V_{DD} = 3.0 V.

Timekeeping mode. Typical I_{DD} as a function of temperature:



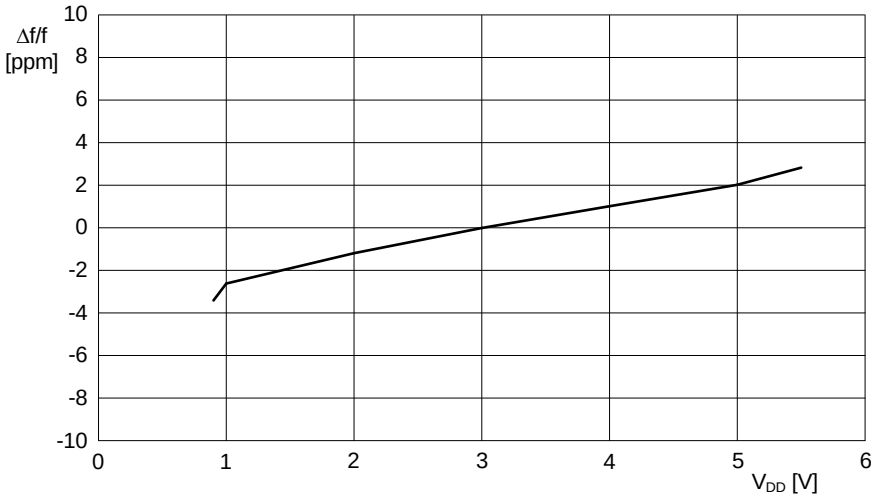
CLKOUT disabled.
(1) V_{DD} = 5.5 V.
(2) V_{DD} = 3.0 V.

Timekeeping mode. Typical I_{DD} with respect to V_{DD}:



T_A = 25°C; timer clock frequency = 1/60 Hz; CLKOUT disabled.

Oscillator frequency variation with respect to V_{DD}:



T_A = 25°C, normalized to V_{DD} = 3 V

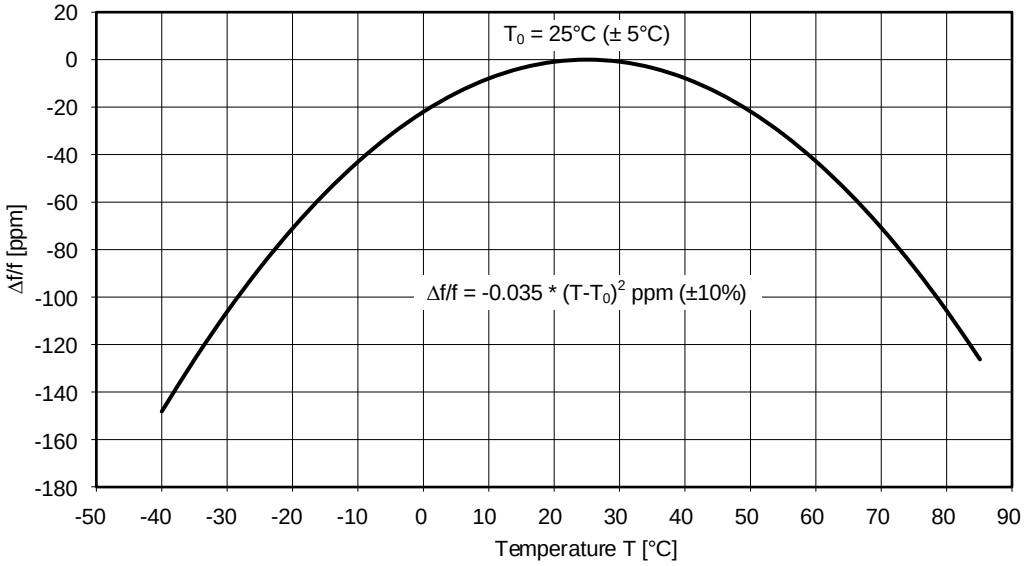
6.3. OSCILLATOR PARAMETERS

For this Table, T_A = -40 to +85°C unless otherwise indicated. V_{DD} = 0.9 to 5.5 V, TYP values at 25°C and 3.0 V.

Oscillator Parameters:

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Xtal General						
f	Crystal Frequency			32.768		kHz
t_{START}	Oscillator start-up time			0.2	2	s
δ_{CLKOUT}	CLKOUT duty cycle	F_{CLKOUT} = 32.768 kHz T_A = 25°C	40		60	%
Xtal Frequency Characteristics						
Δf/f	Frequency accuracy	F = 32.768 kHz T_A = 25°C, V_{DD} = 3.0 V		±10	±20	ppm
Δf/V	Frequency vs. voltage characteristics			±1		ppm/V
$\Delta f/f_{TOPR}$	Frequency vs. temperature characteristics	T_{OPR} = -40°C to +85°C V_{DD} = 3.0 V	$-0.035^{ppm}/_{°C^2}$ $(T_{OPR}-T_0)^2$ ±10%			ppm
T_0	Turnover temperature		20		30	°C
Δf/f	Aging first year max.	T_A = 25°C, V_{DD} = 3.0 V			±3	ppm
Frequency Offset Compensation						
Δt/t	OFFSET value when MODE = 0: Min. comp. step (LSB) and Max. comp. range	T_A = -40°C to +85°C	±4.34		+273.4/ -277.8	ppm
Δt/t	OFFSET value when MODE = 1: Min. comp. step (LSB) and Max. comp. range	T_A = -40°C to +85°C	±4.069		+256.3/ -260.4	ppm
Δt/t	Achievable time accuracy	Calibrated at an initial temperature and voltage	-2.17		+2.17	ppm

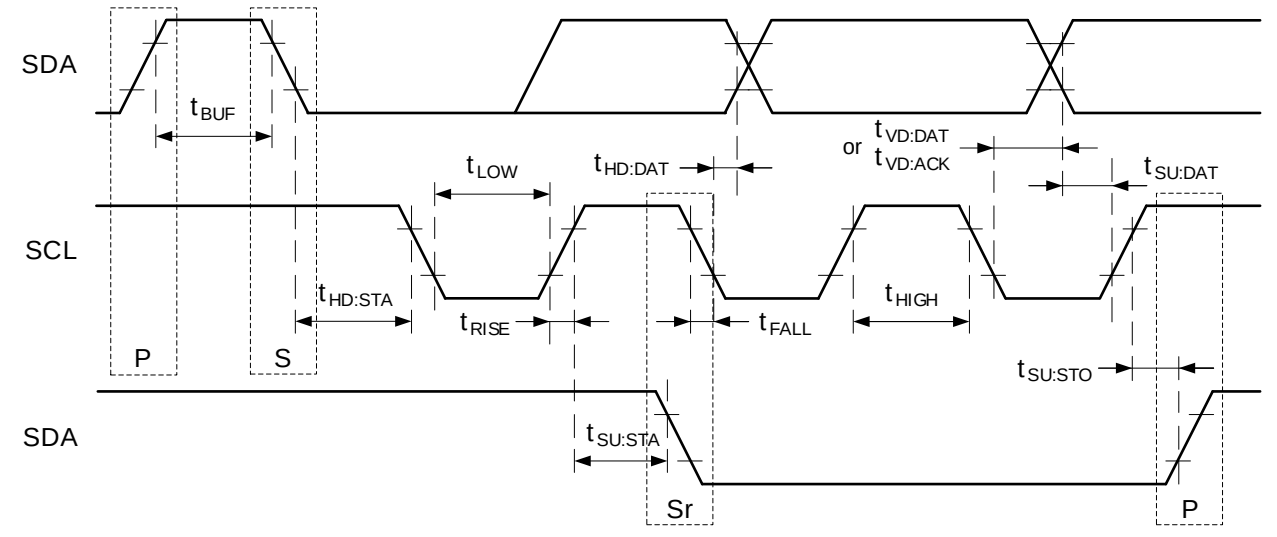
6.3.1.XTAL FREQUENCY VS. TEMPERATURE CHARACTERISTICS



6.4. I²C-BUS CHARACTERISTICS

The following Figure and Table describe the I²C AC electrical parameters.

I²C AC Parameter Definitions:



For the following Table, V_{DD} = 1.8 to 5.5 V, T_A = -40°C to +85°C.

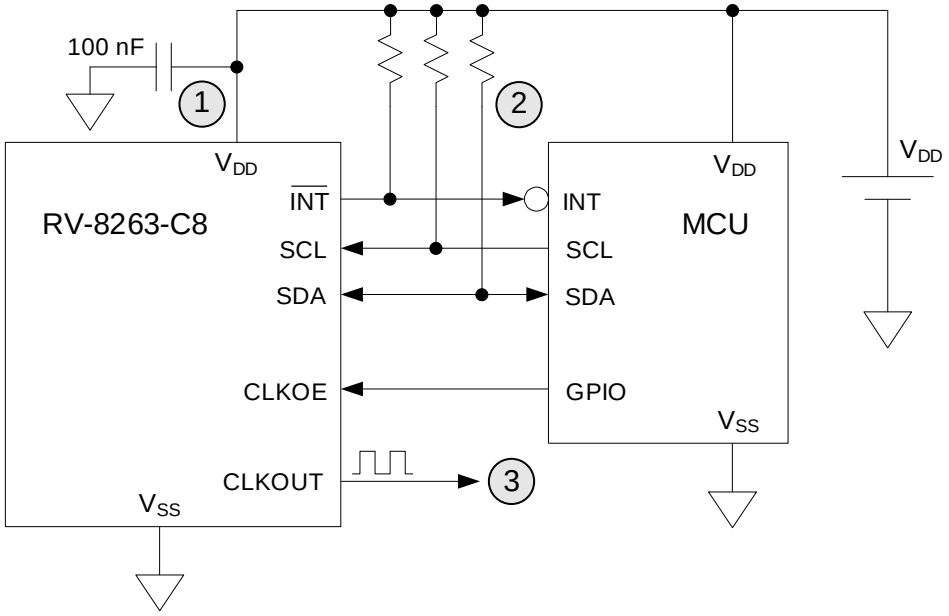
I²C AC Electrical Parameters:

SYMBOL	PARAMETER	MIN	MAX	UNIT
f_{SCL}	SCL input clock frequency	0	400	kHz
t_{LOW}	Low period of SCL clock	1.3		µs
t_{HIGH}	High period of SCL clock	0.6		µs
t_{RISE}	Rise time of SDA and SCL	20	300	ns
t_{FALL}	Fall time of SDA and SCL	20 x (V_{DD} / 5.5 V)	300	ns
$t_{HD:STA}$	START condition hold time	0.6		µs
$t_{SU:STA}$	START condition setup time	0.6		µs
$t_{SU:DAT}$	SDA setup time	100		ns
$t_{HD:DAT}$	SDA hold time	0		µs
$t_{SU:STO}$	STOP condition setup time	0.6		µs
t_{BUF}	Bus free time before a new transmission	1.3		µs
$t_{VD:DAT}$	Data valid time	0	0.9	µs
$t_{VD:ACK}$	Data valid acknowledge time	0	0.9	µs
t_{SP}	Spike pulse width	0	50	ns
C_b	Capacitive load for each bus line		400	pF
S = Start condition, Sr = Repeated Start condition, P = Stop condition				

Caution:
When communicating with the RV-8263-C8 module, the series of operations from transmitting the START (or repeated START) condition to transmitting the STOP (or repeated START) condition should occur within 1 second. If this series of operations requires 1 second or more, the I²C-bus interface will be automatically cleared and set to standby mode by the bus timeout function of the RV-8263-C8 module.

7. APPLICATION INFORMATION

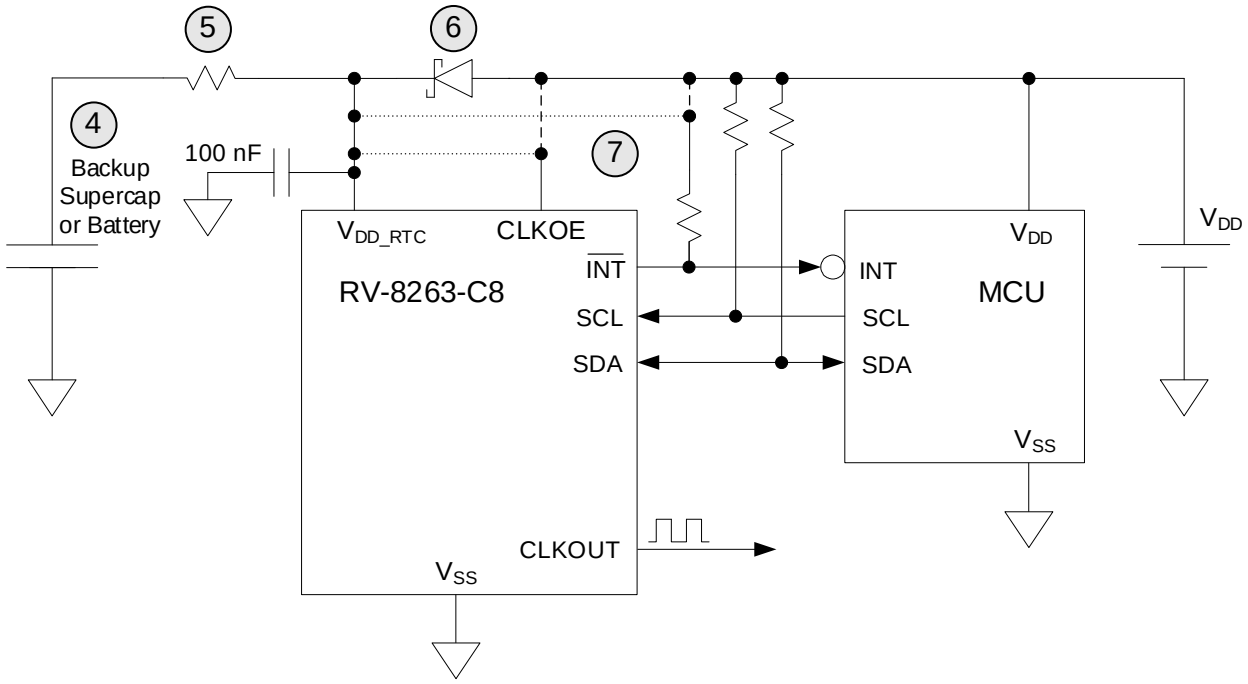
7.1. OPERATING RV-8263-C8



1. A 100 nF decoupling capacitor is recommended close to the device.
2. The $\overline{INT}$ output is an open drain and requires a pull-up resistor to V_{DD}.
3. CLKOUT offers selectable frequencies from 32.768 kHz to 1 Hz for application use. If not used, it is recommended to disable CLKOUT for optimized current consumption by setting FD to 111b or by pulling CLKOE LOW. When disabled, the CLKOUT is LOW.
   Further current minimization can be achieved by turn off the timer (TE = 0) and setting the timer clock frequency to 1/60 Hz (TD = 11b).

7.2. OPERATING RV-8263-C8 WITH BACKUP CAPACITOR

An external diode-circuitry can be wired to ensure standby or back-up supply. With the RTC in its minimum power configuration (see OPERATING RV-8263-C8) the RTC with a supercapacitor may operate for weeks and with a battery for years.



4 Supercapacitor (e.g. 1 farad), primary battery or secondary battery LMR (respect manufacturer specifications for constant charging voltage).

5 When using a supercapacitor, a resistor is used to limit the inrush current into the supercapacitor at power-on. E.g. to comply with the maximum forward current of the schottky diode.
or
When using a battery, a resistor is used to limit the maximum current in case of a short circuit.

6 Schottky diode. This low V_F diode (less than 0.3 V) is needed to not exceed the specified maximum voltage at the inputs of the RV-8263-C8 when normal supply voltage V_{DD} is present ($V_{I\_MAX} = V_{DD\_RTC}$ +0.5 V). Schottky diodes have considerable leakage currents. To optimize backup time it is recommended to select a low leakage Schottky (e.g. BAS70-05).

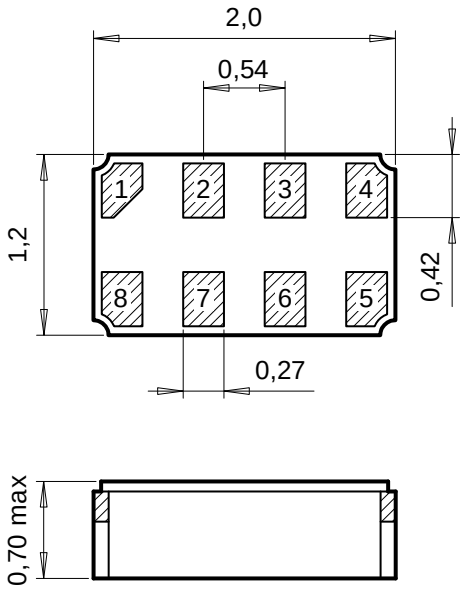
7 If the clock signal (pin CLKOUT) and/or the interrupt signal (pin $\overline{INT}$) are required in backup mode (V_{DD_RTC}) the CLKOE pin and/or the pull-up resistor for the $\overline{INT}$ pin have to be connected to V_{DD_RTC}.

8. PACKAGE

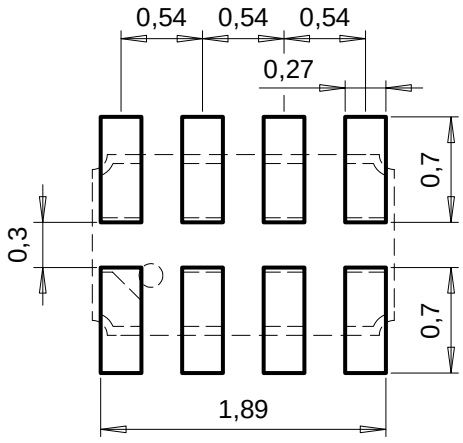
8.1. DIMENSIONS AND SOLDER PAD LAYOUT

RV-8263-C8 Package:

Package dimensions (bottom view):



Recommended solder pad layout:



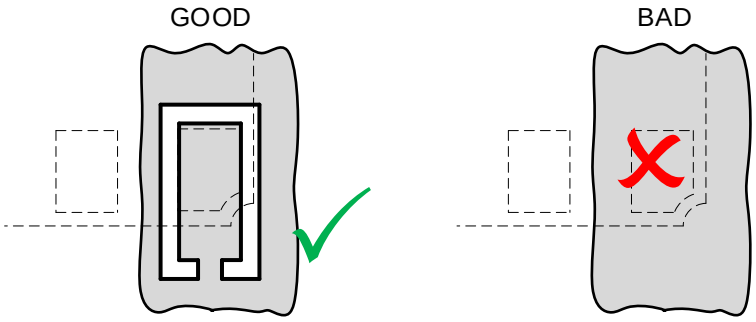
Metal lid is connected to V_{SS} (pin #4)

Dimensions: in mm
Tolerances: unless otherwise specified ±0.1 mm
Drawing: RV-8263-C8_Pack-drw_20230623

8.1.1.RECOMMENDED THERMAL RELIEF

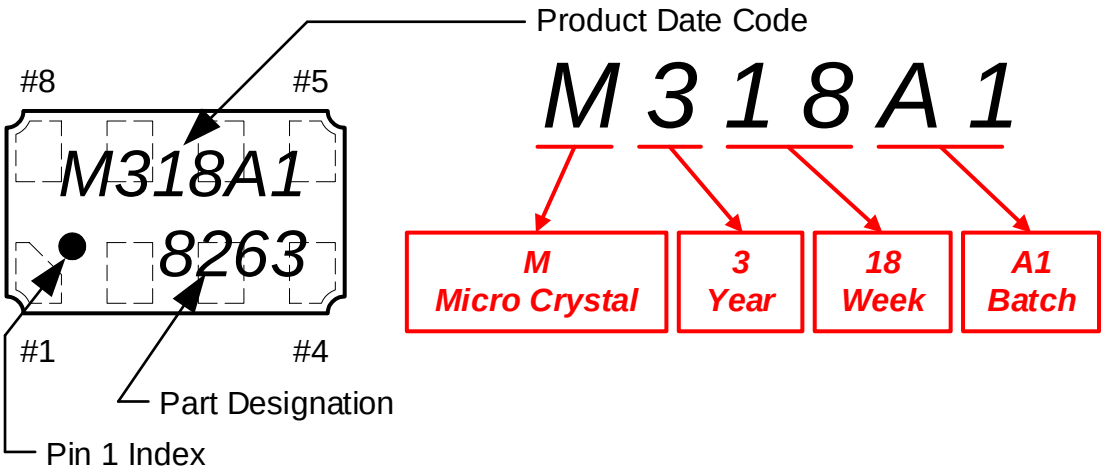
When connecting a pad to a copper plane, thermal relief is recommended.

RV-C8 Package:



8.2. MARKING AND PIN #1 INDEX

Laser marking RV-8263-C8 Package: (top view)

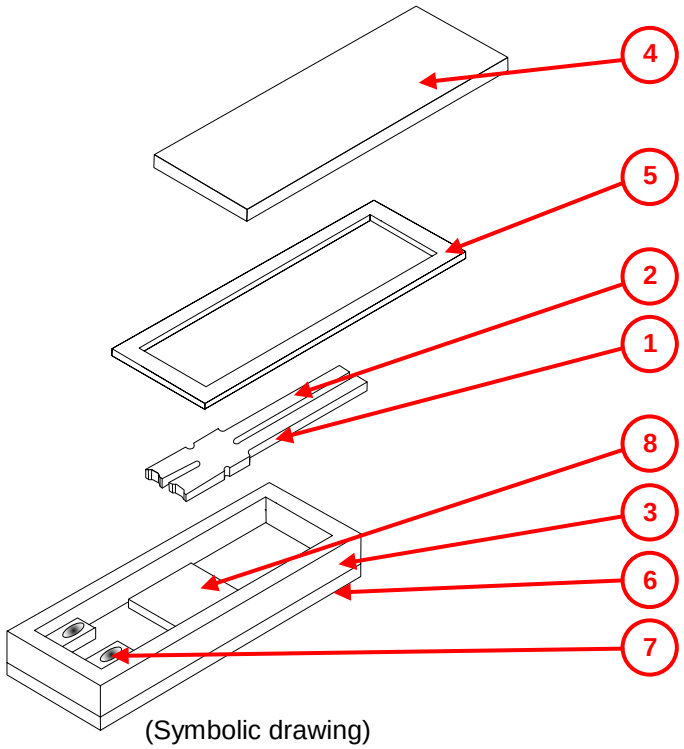


9. MATERIAL COMPOSITION DECLARATION & ENVIRONMENTAL INFORMATION

9.1. HOMOGENOUS MATERIAL COMPOSITION DECLARATION

Homogenous material information according to IPC-1752 standard

Material Composition RV-8263-C8:



(Symbolic drawing)

No.	Item Component Name	Sub Item Material Name	Material Weight (mg)	(%)	Substance Element	CAS Number	Comment
1	Resonator	Quartz Crystal	0.099	100%	SiO_2	14808-60-7	
2	Electrodes	Cr+Au	0.0035	3%	Cr	Cr: 7440-47-3	
				97%	Au	Au: 7440-57-5	
3	Housing	Ceramic	2.92	100%	Al_2O_3	1344-28-1	
4	Metal Lid	Kovar Lid	1.10	91%	Fe53Ni29Co18	Fe: 7439-89-6 Ni: 7440-02-0 Co: 7440-48-4	Metal Lid (Kovar)
		Ni-plating		8.9%	Ni	Ni: 7440-02-0	Nickel plating
		Au-plating		0.1%	Au	Au: 7440-57-5	Gold plating
5	Seal	Solder Preform	0.15	80%	Au80 / Sn20	Au: 7440-57-5	Premelted on Metal Lid
				20%		Sn: 7440-31-5	
6	Terminations	Internal and external terminals	0.48	80%	Mo	Mo: 7439-98-7	Molybdenum
				15%	Ni	Ni: 7440-02-0	Nickel plating
				5%	Au, 0.5 micron	Au: 7440-57-5	Gold plating
7	Resonator attach	Gold bumps	0.011	100%	Au	Au: 7440-57-5	
8	CMOS IC	Silicon	0.29	90%	Si	Si: 7440-21-3	
		Gold bumps		10%	Au	Au: 7440-57-5	
		Unit weight	5.05				

9.2. MATERIAL ANALYSIS & TEST RESULTS

Homogenous material information according to IPC-1752 standard

No.	Item Component Name	Sub Item Material Name	RoHS						Halogens				Phthalates			
			Pb	Cd	Hg	Cr(VI)	PBB	PBDE	F	Cl	Br	I	BBP	DBP	DEHP	DIBP
1	Resonator	Quartz Crystal	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd
2	Electrodes	Cr+Au	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd
3	Housing	Ceramic	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd
4	Metal Lid	Kovar Lid & Plating	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd
5	Seal	Solder Preform	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd
6	Terminations	Int. & ext. terminals	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd
7	Resonator attach	Gold bumps	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd
8	CMOS IC	Silicon & Gold bumps	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd	nd
	MDL [ppm]	Method Detection Limit	2			8	5		50				50			

nd (not detected) = below “Method Detection Limit” (MDL)

Test methods:

RoHS Test method with reference to:

- Pb, Cd IEC 62321-5:2013 MDL: 2 ppm
- Hg IEC 62321-4:2013 + AMD1:2017 MDL: 2 ppm
- Cr(VI) IEC 62321-7-2:2017 MDL: 8 ppm
- PBB / PBDE IEC 62321-6:2015 MDL: 5 ppm

Halogens Test method with reference to BS EN 14582:2016 MDL: 50 ppm

Phthalates Test method with reference to IEC 62321-8:2017 MDL: 50 ppm

9.3. RECYCLING MATERIAL INFORMATION

Recycling material information according to IPC-1752 standard.
Element weight is accumulated and referenced to the unit weight of 5.05 mg.

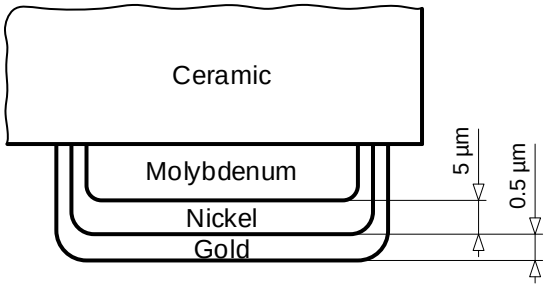
Item Material Name	No.	Item Component Name	Material Weight (mg)	Material Weight (%)	Substance Element	CAS Number	Comment
Quartz Crystal	1	Resonator	0.099	1.96	SiO_2	14808-60-7	
Chromium	2	Electrodes	0.0001	0.002	Cr	Cr: 7440-47-3	
Ceramic	3	Housing	2.92	57.78	Al_2O_3	1344-28-1	
Gold	2 4 5 6 7 8	Electrodes Metal Lid Seal Terminations Resonator attach CMOS IC	0.19	3.73	Au	Au: 7440-57-5	
Tin	5	Seal	0.03	0.59	Sn	Sn: 7440-31-5	
Nickel	4 6	Metal Lid Terminations	0.17	3.36	Ni	Ni: 7440-02-0	
Molybdenum	6	Terminations	0.38	7.60	Mo	Mo: 7439-98-7	
Kovar	4	Metal Lid	1.00	19.81	Fe53Ni29Co18	Fe: 7439-89-6 Ni: 7440-02-0 Co: 7440-48-4	
Silicon	8	CMOS IC	0.26	5.16	Si	Si: 7440-21-3	
	Unit weight (total)		5.05	100			

9.4. ENVIRONMENTAL PROPERTIES & ABSOLUTE MAXIMUM RATINGS

Package	Description
SON-8 ceramic package	Small Outline Non-leaded (SON), hermetically sealed ceramic package with metal lid

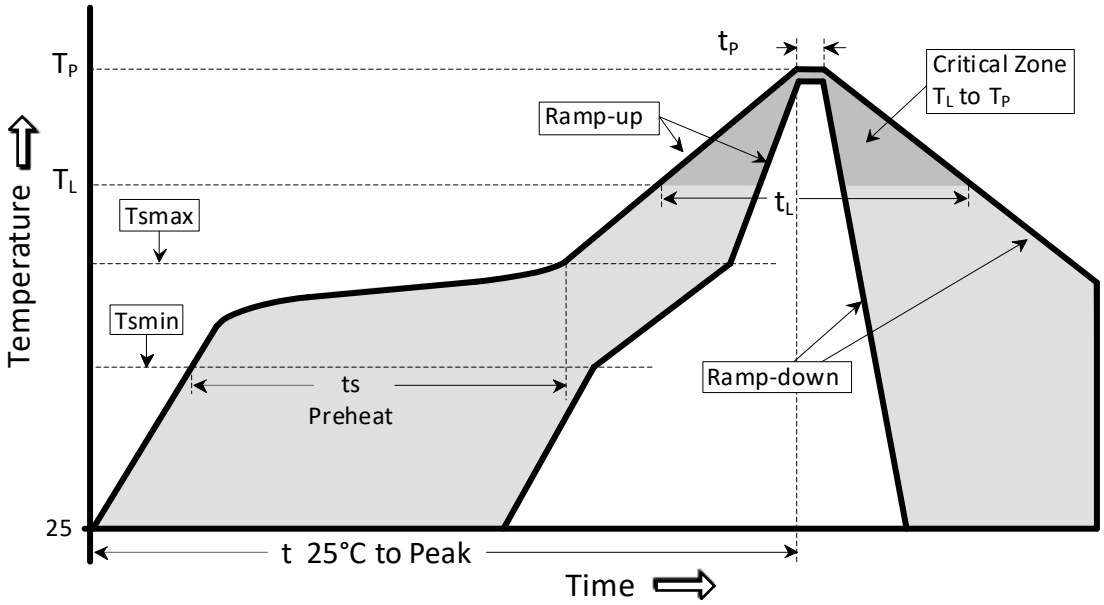
Parameter	Directive	Conditions	Value
Product weight (total)			5.05 mg
Storage temperature		Store as bare product	-55 to +125°C
Moisture sensitivity level (MSL)	IPC/JEDEC J-STD-020D		MSL1
FIT / MTBF			available on request

Terminal finish:



10. SOLDERING INFORMATION

Maximum Reflow Conditions in accordance with IPC/JEDEC J-STD-020C "Pb-free"



Temperature Profile	Symbol	Condition	Unit
Average ramp-up rate	(Ts_{max} to T_P)	3°C / second max	°C / s
Ramp down Rate	T_{cool}	6°C / second max	°C / s
Time 25°C to Peak Temperature	$T_{to\text{-}peak}$	8 minutes max	min
Preheat			
Temperature min	Ts_{min}	150	°C
Temperature max	Ts_{max}	200	°C
Time Ts_{min} to Ts_{max}	ts	60 – 180	sec
Soldering above liquidus			
Temperature liquidus	T_L	217	°C
Time above liquidus	t_L	60 – 150	sec
Peak temperature			
Peak Temperature	Tp	260	°C
Time within 5°C of peak temperature	tp	20 – 40	sec

11. HANDLING PRECAUTIONS FOR MODULES WITH EMBEDDED CRYSTALS

The built-in tuning-fork crystal consists of pure Silicon Dioxide in crystalline form. The cavity inside the package is evacuated and hermetically sealed in order for the crystal blank to function undisturbed from air molecules, humidity and other influences.

Shock and vibration:

Keep the crystal / module from being exposed to **excessive mechanical shock and vibration**. Micro Crystal guarantees that the crystal / module will bear a mechanical shock of 5000 g / 0.3 ms.

The following special situations may generate either shock or vibration:

Multiple PCB panels - Usually at the end of the pick & place process the single PCBs are cut out with a router. These machines sometimes generate vibrations on the PCB that have a fundamental or harmonic frequency close to 32.768 kHz. This might cause breakage of crystal blanks due to resonance. Router speed should be adjusted to avoid resonant vibration.

Ultrasonic cleaning - Avoid cleaning processes using ultrasonic energy. These processes can damage the crystals due to the mechanical resonance frequencies of the crystal blank.

Overheating, rework high temperature exposure:

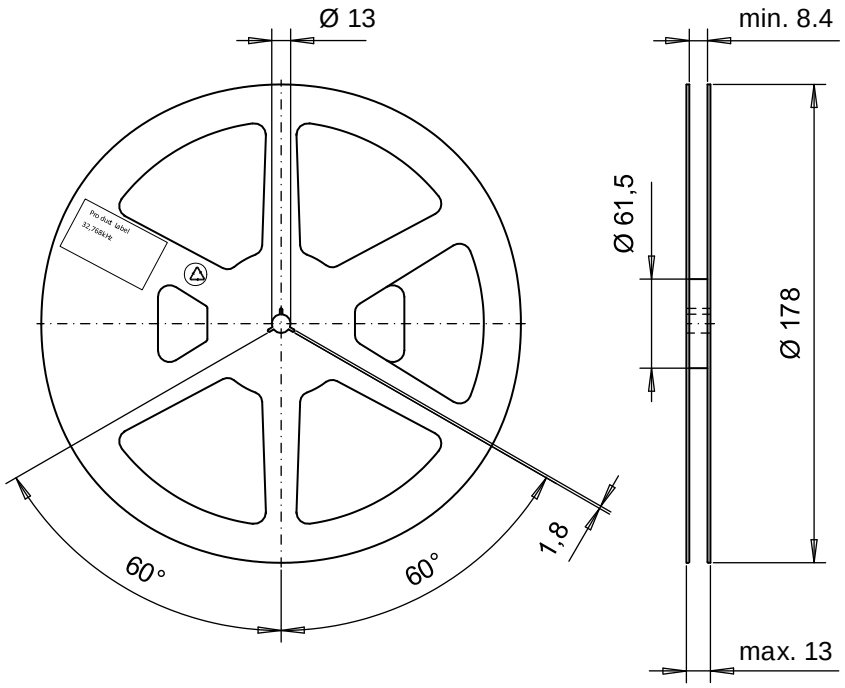
Avoid overheating the package. The package is sealed with a seal ring consisting of 80% Gold and 20% Tin. The eutectic melting temperature of this alloy is at 280°C. Heating the seal ring up to >280°C will cause melting of the metal seal which then, due to the vacuum, is sucked into the cavity forming an air duct. This happens when using hot-air-gun set at temperatures >280°C.

Use the following methods for rework:

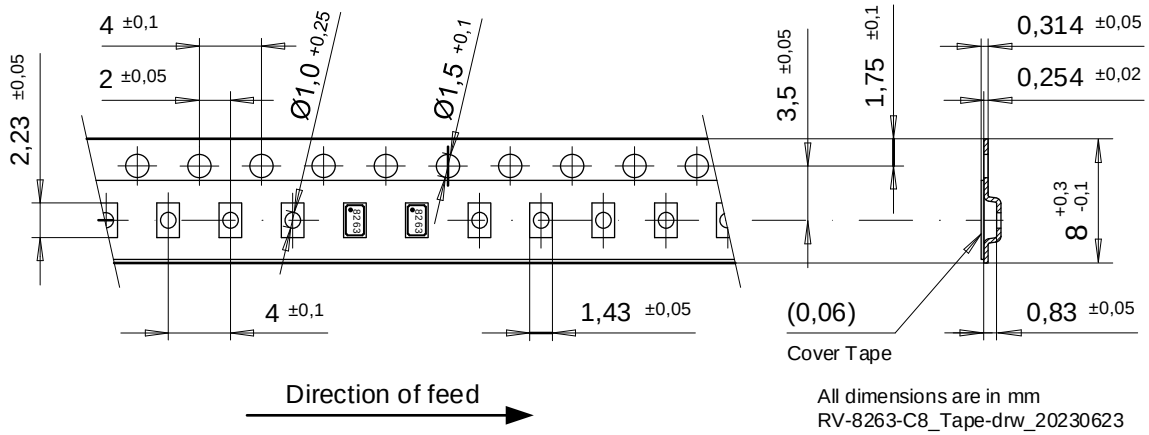
- Use a hot-air-gun set at 270°C.
- Use 2 temperature controlled soldering irons, set at 270°C, with special-tips to contact all solder-joints from both sides of the package at the same time, remove part with tweezers when pad solder is liquid.

12. PACKING & SHIPPING INFORMATION

Reel: 7” = 178 mm



Carrier Tape:
Material: Polycarbonate, conductive
Width: 8 mm
Tape Leader and Trailer: Minimum length 300 mm



Cover Tape:
Tape: Polypropylene, 3M™ Universal Cover Tape (UCT)
Adhesive Type: Pressure sensitive, Synthetic Polymer
Thickness: 0.06 mm

Peel Method:
Medial section removal, both lateral stripes remain on carrier

13. COMPLIANCE INFORMATION

Micro Crystal confirms that the standard product Real-Time Clock Module RV-8263-C8 is compliant with “EU RoHS Directive” and “EU REACh Directives”.
Please find the actual Certificate of Conformance for Environmental Regulations on our website:
CoC_Environment_RV-Series.pdf

14. DOCUMENT REVISION HISTORY

Date	Revision #	Revision Details
June 2023	1.0	First release

MICRO CRYSTAL SWITZERLAND
A COMPANY OF THE SWATCH GROUP

Micro Crystal AG
Muehlestrasse 14
CH-2540 Grenchen
Switzerland

Phone +41 32 655 82 82
sales@microcrystal.com
www.microcrystal.com